

Unidirectional Switch-Boxes for Synthesizable Reconfigurable Arrays

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1. Introduction

The new trend in designing reconfigurable Systems-on-Chip (SoC) by using embedded FPGAs provides numerous improvements to ASIC designs due to the added flexibility and improvements in functionality. Further advantages are introduced if the FPGA is provided as a synthesizable core that fits well in the SoC architecture and design flow. Such synthesizable reconfigurable arrays have been proposed earlier by the authors in [1] and [2]; the arrays are provided as synthesizable soft-cores to make them fully customizable at design-time to tune the array to the desired application domain. As described in [3] and [4], providing the arrays as synthesizable cores greatly simplifies the integration of the array in the SoC software flow.

The described arrays used a mesh-based interconnect architecture [7]. It was measured that in the case of synthesizable arrays that programmable interconnects occupied up to 90% of the total array area and 91% of the total power consumption [2]. Furthermore, around 42% of the total area and power is consumed by the switch-boxes [7] in the mesh. The inefficiency occurs when trying to build synthesizable interconnects having the same functionality as typical interconnects found in FPGAs. Programmable switches used in FPGAs are based on simple pass-transistors; Implementing a switch with the same functionality using standard-cell libraries requires the use of two tri-state buffers which represents an 8 times increase in area over a single transistor.

This paper proposes and investigates different designs of Switch-boxes suitable for synthesis in reconfigurable coarse-grain architectures. The various designs are evaluated and compared in terms of power consumption, area, delays and routability.

Published work on switch-box design is mainly concentrated on non-synthesizable circuit designs of switches. Synthesizable interconnects were presented in [3] and [4] for small embedded arrays; the arrays are designed for small combinatorial logic such as next-state circuits. The arrays are based on interconnected programmable Look-Up-Tables; interconnects were based on directional switch blocks that allows only left-to-right data flow in order to prevent the occurrence of combinatorial feedback loops. The configurable switches were implemented using tri-state buffers. In [5] several designs were proposed for generic switchboxes, with one multiplexer-based switchbox suitable for synthesis.

2. Proposed Switch-Boxes

Synthesizable programmable switches can be either based on tri-state buffers or on multiplexers. The following four switch designs are evaluated:

- (1) *Full directions using tri-states*
- (2) *Full directions using multiplexers*
- (3) *Reduced directions using tri-states*
- (4) *Reduced directions using multiplexers*

A switch-box with the standard topology (shown in figure 1(f) is constructed with each programmable switch type. It was initially measured that this topology provided better routability than the Universal or Wilton topologies [8], however, the switch design can be used for any other topology depending on the application.

To form a bidirectional programmable switch two tri-state buffers are required, as shown in fig. 1(a). The same switchbox structure can be achieved by using multiplexers as in fig. 1(b). It is also possible to reduce the required number of switches by using only unidirectional switches, as in fig. 1(c)-1(h).

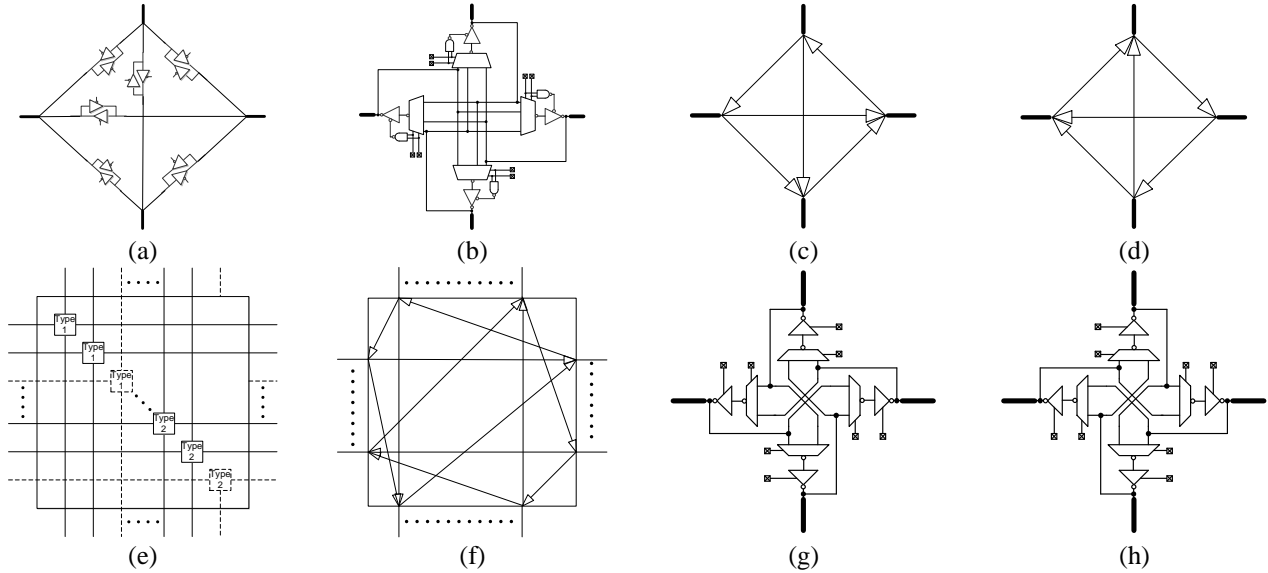


Figure 1: (a): Switch using tri-state buffers. (b): Switch using 3-to-1 multiplexers and buffers. (c), (d): Two possible types of unidirectional switches. (e): Combining the two types of switches in an S-box, and (e) is the resulting S-Box topology. (g), (h): Unidirectional switches using 2-to-1 multiplexers.

3. Performance Evaluation

The four switches are evaluated and compared in terms of area, power consumption, delays and routability. A benchmark DCT circuit [2] is used to measure the performance of each switch box used in a domain-specific array for distributed arithmetic [2]. The array uses 12 1-bit tracks and 12 4-bit tracks. The area, power and delays of the whole array running the DCT algorithm is measure using standard ASIC software. The routability of the switch-boxes is found using a modified version of the standard FPGA place and route tool VPR [9]. The program was modified to support heterogeneous coarse-grain clusters, as well as word-wide interconnects.

It should be noted that the area of switch-boxes depends on two factors: the area needed for the programmable switches and the one needed to store the configuration memory. Reducing the number of configuration bits is crucial, since the memory cells occupy up to 60% of the total area. These figures suppose the use of flip-flops, which have the highest area occupancy among synthesizable memory elements. The power consumption depends on the overall switching activity in the array and on the overall wirelength of the routings. Similarly, the delays are related to the overall wirelength and to the delays inside the switching elements of the boxes (e.g. multiplexers and tri-state buffers).

It can be seen from figure 2 that the use of multiplexers in (2) and (6) is not efficient when compared to (1) and (4), as power is increased up to 29% due to the power

consumed by multiplexers and the loading effect. This figure is only 8% percent between (6) and (4) since 2-to-1 multiplexers are used. Similarly, delays are 37% longer when using multiplexers. The area of the multiplexers-based switches is only 5.2% higher; this is due to the fact that the multiplexers have a higher area than buffers but require a lower number of configuration bits. As expected, the unidirectional switches (3) and (4) have around 53% the area of the full switches (1) and (2), and at the same time they provide a 27% decrease in power consumption, due to the reduce load on the tracks. This comes at the cost of reduced routability since the wirelength is increased by 12%, which in turn increases the delays by 7%.

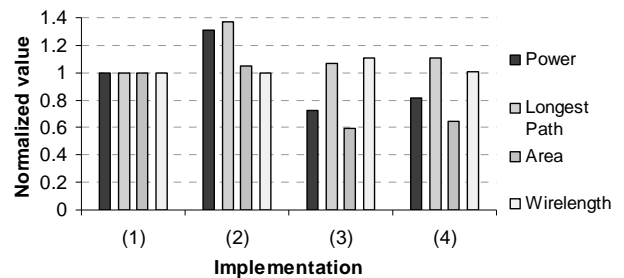


Figure 2: Performance of the proposed switch-boxes in terms of power consumption, area, delays and routability

From the above analysis we can conclude that a unidirectional switch-box based on tri-state buffers provides up to 22% power and 47% area reductions when

compared to the bidirectional alternative, at the expense of an increase of only 10% in delays and wirelength.

4. References

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