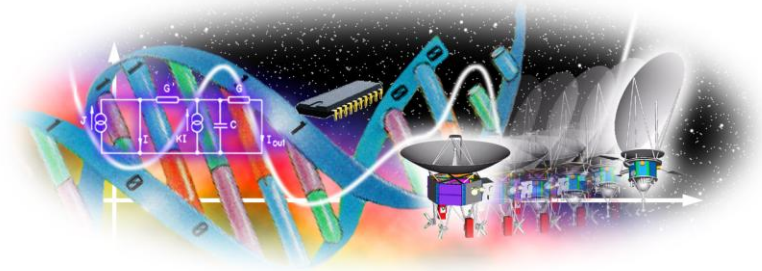


# 2009 NASA/ESA Conference on Adaptive Hardware and Systems



*July 29 – August 1, 2009  
Moscone Convention Center  
San Francisco, California, USA*

**Organized by**

NASA Jet Propulsion Laboratory (JPL), European Space Agency (ESA),  
University of Edinburgh, UK

**Supported by**

IEEE Circuits and Systems Society (IEEE-CAS)  
Society for Adaptive and Evolvable Hardware and Systems (ADEVO)  
Bio-Inspired Technologies and Systems (BITS),-JPL  
European Centre for Secure Information and Systems (ECSIS)

**General Chair**

*Martin Suess, European Space Agency, The Netherlands*

**Vice General Chairs**

*Tughrul Arslan, University of Edinburgh, UK  
Didier Keymeulen, Jet Propulsion Laboratory, USA*



WEDNESDAY, JULY 29, 2009

TUTORIALS

*Chairs: Didier Keymeulen, Jet Propulsion Laboratory (JPL), USA  
Ahmet T. Erdogan, University of Edinburgh, UK  
Room 304*

08:00 – 08:45

Registration  
North Lobby

08:45 – 09:45  
Room 304

**Tutorial 1: Evolvable Hardware**  
Jim Torresen, *University of Oslo, Norway*  
Lukas Sekanina, *Brno University of Technology, Czech Republic*

09:45 – 10:00

BREAK 1  
Room 307

10:00 - 11:00

**Tutorial 2: On-Die Calibration and Self-Correction Approaches for Reliable Clock Distribution Networks of High Performance Microprocessors**  
Cecilia Metra, *University of Bologna, Italy*  
Simon Tam, *Intel Corporation's Enterprise Microprocessors Group, USA*  
TM Mak, *Intel Corporation's Sort/Test Technology Development Group, USA*

11:00 - 11:15

BREAK 2  
Room 307

11:15 - 12:15

**DAC Keynote: The End of Denial Architecture and the Rise of Throughput Computing**  
William J. Dally  
*NVIDIA Corp. and Stanford University, USA*  
*Gateway Ballroom (for "DAC Exhibition-only" registrants)*

12:15 - 14:00

LUNCH and DAC Exhibition (*on your own*)

14:00 – 15:00

**Tutorial 3: Fault Injection Techniques and Tools**  
Massimo Violante  
*Politecnico di Torino, Italy*

15:00 - 15:15

BREAK 3  
Room 307

15:00 – 16:00

**Tutorial 4: Emerging Technologies**  
Christof Teuscher  
*Portland State University, USA*

16:00 – 16:15

BREAK 4  
Room 307

16:15 – 17:15

**Tutorial 5: High Performance FPGA-based Bioinformatics**  
Khaled Benkrid  
*University of Edinburgh, UK*

**THURSDAY, JULY 30, 2009**

TRACK I Room 304		TRACK II Room 305	
08:00 - 09:00	Conference Registration North Lobby		
09:00 - 09:15	<p align="center"><b>Welcome Address and Organizational Remarks (Room 304)</b>                      Philippe Armbruster (European Space Agency – ESA), Didier Keymeulen (Jet Propulsion Laboratory - JPL) and Tughrul Arslan (University of Edinburgh)</p>		
09:15 - 10:00	<p align="center"><b>Invited Keynote Address (Room 304): Robotics Technology for Space Exploration Missions</b>                      Richard Volpe                      Manager of the Mobility and Robotics Systems Section, Autonomous Systems Division,                      Jet Propulsion Laboratory, USA                      Chair: Adrian Stoica, Jet Propulsion Laboratory (JPL), USA</p>		
10:00 - 10:20	BREAK 1 Room 307		
<p align="center"><b>Session 1A: Reconfigurable Hardware (Part I)</b>                      Chair: David Merodio                      European Space Agency (ESA), The Netherlands</p>		<p align="center"><b>Session 2A: Evolvable Hardware (Part I)</b>                      Chair: Didier Keymeulen                      Jet Propulsion Laboratory (JPL), USA</p>	
10:20 - 10:45	Dynamically Adapted Low-Energy Fault Tolerant Processors Monica Magalhães Pereira, Luigi Carro, Federal University of Rio Grande do Sul	A Multi-cellular Developmental Representation for Evolution of Adaptive Spiking Neural Microcircuits in FPGA Hooman Shayani, Peter J. Bentley, UCL Andy M. Tyrrell, University of York	
10:45 - 11:10	Partial Bitstream 2-D Core Relocation for Reconfigurable Architectures Chad Rossmeyssil, Adarsha Sreeramreddy, Ali Akoglu, University of Arizona	EvoCaches: Application-specific Adaptation of Cache Mappings Paul Kaufmann, Christian Plessl, Marco Platzner, University of Paderborn	
11:10 - 11:35	Defect tolerance of an optically reconfigurable gate array with a one-time writable volume holographic memory Takayuki Mabuchi, Kenji Miyashiro, Minoru Watanabe, Akifumi Ogiwara, Shizuoka University	Intermediate Level FPGA Reconfiguration for an Online EHW Pattern Recognition System Kyrre Glette, Jim Torresen, Mats Hovin, University of Oslo	
11:35 - 12:00	Implementation of Highly Pipelined Datapaths on a Reconfigurable Asynchronous Substrate Khodor Fawaz, Tughrul Arslan, Iain Lindsay, University of Edinburgh	Evolution of Impulse Burst Noise Filters Zdenek Vasicek, Michal Bidlo, Lukas Sekanina, Faculty of Information Technology, Brno University of Technology Jim Torresen, Kyrre Glette, University of Oslo	
12:00-14:00	LUNCH and DAC Exhibition (on your own)		
<p align="center"><b>Session 1B: Special Session on Emerging Computer Technologies for Adaptive Systems</b>                      Organiser and Chair: Khaled Benkrid                      University of Edinburgh, UK</p>		<p align="center"><b>Session 2B: Embryonic Hardware and Morphogenesis</b>                      Chair: Adrian Stoica                      Jet Propulsion Laboratory (JPL), USA</p>	
14:00-14:25	Accelerating Phase Correlation functions using GPUs and FPGAs: A comparison study Kentaro Matsuo, Tsuyoshi Hamada, Masayuki Miyoshi, Yuichiro Shibata, Kiyoshi Oguri, Nagasaki University	eDNA: A Bio-Inspired Reconfigurable Hardware Cell Architecture Supporting Self-organisation and Self-healing Michael Reibel Boesen, Jan Madsen, Technical University of Denmark	
14:25- 14:50	Performance Analysis of IBM Cell Broadband Engine on Sequence Alignment Yang Song, Gregory M. Striemer, Ali Akoglu, University of Arizona	Self-Testable and Self-Repairable Bio-Inspired Configurable Circuits Andre Stauffer, Joel Rossier, Ecole polytechnique fédérale de Lausanne (EPFL)	
14:50 - 15:15	A comparative study on ASIC, FPGAs, GPUs and general purpose processors in the O(N <sup>2</sup> ) gravitational N-body simulation Tsuyoshi Hamada, Khaled Benkrid, Keigo Nitadori, Makoto Taiji, Nagasaki University	Prokaryotic Bio-Inspired Model for Embryonics Mohammad Samie, Gabriel Dragffy, Anca Popescu, Tony Pipe, Chris Melhuish, University of the West of England, UWE	
15:15-15:45	BREAK 2 Room 307		
15:45-16:10	GP-GPU: Bridging the Gap between Modelling & Experimentation Thomas F. Clayton, Alan F. Murray, Iain Lindsay, University of Edinburgh	Prokaryotic Bio-Inspired System Mohammad Samie, Gabriel Dragffy, Anca Popescu, Tony Pipe, Janice Kiely, University of the West of England, UWE	
<p align="center"><b>Session 1C: Adaptive Antennas</b>                      Chair: Tughrul Arslan                      University of Edinburgh, UK</p>		<p align="center"><b>Session 2C: Application of Adaptive Systems</b>                      Chair: Andy Tyrrell                      The University of York, UK</p>	
16:10-16:35	A Substrate Integrated Fluidic Compensation Mechanism for Deformable Antennas Gregory Huff, Stephen Long, Texas A&M University	On-Board Vision Processing for Small UAVs: Time to Rethink Strategy Shoaib Ehsan, Klaus D. McDonald-Maier, University of Essex	
16:35-17:00	Effect of a Central Antenna Element on the Directivity, Half-Power Beamwidth and Side-Lobe Level of Circular Antenna Arrays Virgilio Zuniga, Nakul Haridas, Ahmet T. Erdogan, Tughrul Arslan, University of Edinburgh	Please go to Session 1C in Track I	
17:30 - 19:30	<p align="center"><b>Reception and Posters</b>                      Room 307                      Chair: Ahmet T. Erdogan, University of Edinburgh, UK</p>		
Poster 1	Selective Triple Modular Redundancy for Single Event Upset (SEU) Mitigation Xiaoxuan She, State Key Laboratory of ASIC & System, Fudan University		
Poster 2	Scheduling Temporal Partitions in a Multiprocessing Paradigm for Reconfigurable Architectures Andreas Popp, Yannick Le Moulec, Peter Koch, Aalborg University		
Poster 3	A Fingerprint Identification System using adaptive FPGA-based Enhanced Probabilistic Convergent Network Pierre Lorrent, Gareth Howells, University of Kent, Klaus McDonald-Maier, University of Essex		
Poster 4	Integrating Feature Values for Key Generation in an IC Metric System Evangelos Papoutsis, Gareth Howells, Department of Electronics - University of Kent at Canterbury Andrew Hopkins, Klaus McDonald-Maier, School of Computer Science and Electronics Engineering – University of Essex		
Poster 5	Evolutionary Algorithms in Unreliable Memory Haisoo Shin, Yun-Geun Lee, Bob McKay, Nguyen Xuan Hoai, Seoul National University		
Poster 6	Implementation of an IEEE802.11a Transmitter for a Reconfigurable System-on-a-Chip Design Tanya Vladimirova, Jean Robert Paul, University of Surrey		
Poster 7	MORA – An Architecture and Programming Model for a Resource Efficient Coarse Grained Reconfigurable Processor Sai Rahul Chalamalasetti, Sohan Purohit, Martin Margala, University of Massachusetts Lowell Wim Vanderbauwhede, University of Glasgow		
Poster 8	Mersenne Twister Random Number Generation on FPGA, CPU and GPU Xiang Tian, Khaled Benkrid, University of Edinburgh		
Poster 9	Conditional Acknowledge Synchronisation in Asynchronous Interconnect Switch Design Khodor Fawaz, Tughrul Arslan, Iain Lindsay, University of Edinburgh		
Demo	Flight Hardware Implementation of Lossless Adaptive Hyperspectral Data Compression for Space Didier Keymeulen, Nazeeh Aranki, Matthew Klimesh, Jet Propulsion Laboratory Alireza Bakhshi, B&A Engineering		

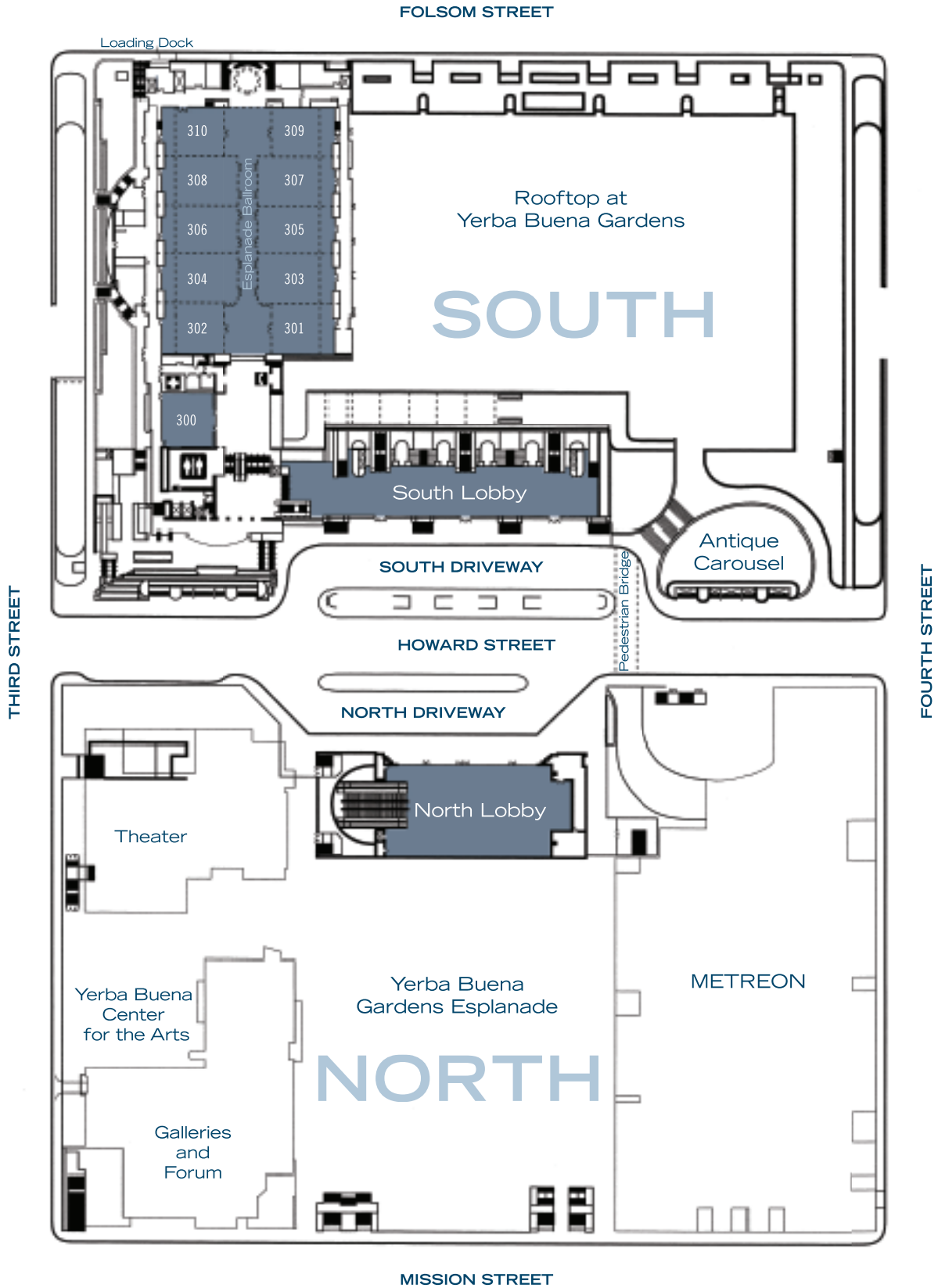
**FRIDAY, JULY 31, 2009**

TRACK I Room 304		TRACK II Room 305	
08:30 - 09:00	Registration North Lobby		
09:00 - 09:45	<p align="center"><b>Invited Keynote Address (Room 304): Adaptive Systems for Space: A Smooth or a Disruptive Evolution?</b></p> <p align="center">Philippe Armbruster Head of the Data System Division, ESTEC, European Space Agency (ESA), The Netherlands</p> <p align="center">Chair: Tughrul Arslan, University of Edinburgh, UK</p>		
09:45 - 10:05	BREAK 1 Room 307		
<p align="center"><b>Session 1D: Reconfigurable Hardware (Part II)</b></p> <p align="center">Chair: David Merodio European Space Agency (ESA), The Netherlands</p>		<p align="center"><b>Session 2D: Evolvable Hardware (Part II)</b></p> <p align="center">Chair: Didier Keymeulen Jet Propulsion Laboratory (JPL), USA</p>	
10:05 - 10:30	A sixteen-context dynamic optically reconfigurable gate array Mao Nakajima, Minoru Watanabe, Shizuoka University	Adapting a genotype-phenotype mapping to phenotypic complexity Morten Hartmann, Norwegian University of Science and Technology Tim Goedeweck, Katholieke Universiteit Leuven	
10:30 - 10:55	An Adaptable Task Manager for Reconfigurable Architecture Kernels Yury Shiyonovskii, Francis Wolff, Chris Papachristou, Case Western Reserve University	Polymorphic FIR Filters with Backup Mode Enabling Power Savings Lukas Sekanina, Richard Ruzicka, Zbysek Gajda, Brno University of Technology	
10:55 - 11:20	A new application-tuned processor architecture for high-performance reconfigurable computing Li-Hong Shang, Mi Zhou, Jiong Zhang, Hong-Bin Li, Beihang University	A Flexible Bit-Stream Level Evolvable Hardware Platform Based on FPGA HuaQiu Yang, LiGuang Chen, ShaoTeng Liu, HaiXiang Bu, JinMei Lai, ASIC & System State Key Lab, Fudan University	
11:20 - 11:45	BREAK 2 Room 307		
<p align="center"><b>Session 1E: Adaptive Wired and Wireless Networks</b></p> <p align="center">Chair: Klaus McDonald-Maier University of Essex, UK</p>		<p align="center"><b>Session 2E: On-Chip Learning and Adaptation</b></p> <p align="center">Chair: Andre Stauffer EPFL, Switzerland</p>	
11:45 - 12:10	Autonomous Configuration Method for Real-Time Location Systems Thorsten Edelh�user, University of Erlangen-Nuremberg Gabriella K�kai, Fraunhofer Institute for Integrated Circuits	Synchronous Digital Implementation of the AER Communication Scheme for Emulating Large-Scale Spiking Neural Networks Models J. Manuel Moreno, Jordi Madrenas, Technical university of Catalunya (UPC), Lukasz Kotynia, Technical University of Lodz	
12:10 - 12:35	Testbed for Node Communication in MANETs to Uniformly Cover Unknown Geographical Terrain Using Genetic Algorithms Cevher Dogan, Cem Safak Sahin, M. Umit Uyar, Elkin Urrea, The City College of the City University of New York	Adaptive Sub-threshold Test Circuit Matthew J. Turnquist, Erka Laulainen, Lauri Koskinen, Helsinki University of Technology Jani Makipaa, VTT, Hannu Tenhunen, University of Turku	
12:35 - 13:00	An Adaptive Energy Efficient Transmission Protocol in Wireless Ad-hoc Network Junjun Gu, Gang Qu, Tianzhou Chen, University of Maryland, College Park Ahmed Bouridane, Queen's University of Belfast	Please go to Session 1E in Track I	
13:00 - 14:00	LUNCH (on your own)		
<p align="center"><b>Session 1E: Adaptive Wired and Wireless Networks (cont.)</b></p> <p align="center">Chair: Klaus McDonald-Maier University of Essex, UK</p>		<p align="center"><b>Session 2F: Adaptive Systems for Space Applications</b></p> <p align="center">Chair: Gianluca Tempesti University of York, UK</p>	
14:00 - 14:25	Direct Reinforcement Learning for Autonomous Power Configuration and Control in Wireless Networks Adrian Udenze, Klaus McDonald-Maier, University of Essex	Flight Hardware Implementation of Lossless Adaptive Hyperspectral Data Compression for Space Applications Didier Keymeulen, Nazeeh Aranki, Matthew Klimesh, Jet Propulsion Laboratory Alireza Bakhshi, B&A Engineering	
14:25 - 14:50	Indirect Reinforcement Learning for Autonomous Power Configuration and Control in Wireless Networks Adrian Udenze, Klaus McDonald-Maier, University of Essex	New Methodology for Reducing Sensor and Readout Electronics Circuitry Noise in Digital Domain Semion Kizhner, NASA Katherine Heinzen, University of Notre Dame	
14:50 - 15:15	<p align="center"><b>Session 2H: Automated Design Methodologies and Tools</b></p> Flexible Datapath Synthesis Through Arithmetically Optimized Operation Chaining Sotirios Xydias, Ioannis Triantafyllou, George Economakos, Kiamal Pekmezci, National Technical University of Athens	Low-Complexity Hyperspectral Image Compression on a Multi-tiled Architecture Karel H.G. Walters, Andre B.J. Kokkeler, Gerard Smit, University of Twente	
15:15 - 15:45	BREAK 3 Room 307		
<p align="center"><b>Session 1F: Special Session on Reconfigurable and Adaptive Multiprocessor Systems-on-Chip</b></p> <p align="center">Organiser and Chair: Giovanni Beltrame, European Space Agency (ESA), The Netherlands</p>		<p align="center"><b>Session 2F: Adaptive Systems for Space Applications (cont.)</b></p> <p align="center">Chair: Gianluca Tempesti University of York, UK</p>	
15:45 - 16:10	Self-optimization of MPSoCs Targeting Resource Efficiency and Fault Tolerance Mario Pormann, Madhura Purnaprajna, Christoph Puttmann, University of Paderborn	Dynamic Partial Reconfiguration in Space Applications Bj�rn Osterloh, Harald Michalik, Bj�rn Fiethe, IDA, Technische Universit�t Braunschweig Sandi Habinc, Aeroflex Gaisler AB	
16:10 - 16:35	Optimizing configuration and application mapping for MPSoC architectures S�bastien Le Beux, Gabriela Nicolescu, Guy Bois, Youcef Bouchebaba, Michel Langevin, Pierre Paulin, Ecole Polytechnique de Montreal	<p align="center"><b>Session 2G: Learning and Evolutionary Algorithms for Adaptive Hardware</b></p> <p align="center">Chair: Jim Torresen University of Oslo, Norway</p>	
16:35 - 17:00	Quality of Service in NoC for Reconfigurable Space Applications Albert Ferrer, Steve Parkes, Peter Mendham, University of Dundee	Stochastic Adaptation to Environmental Changes Supported by Endocrine System Principles Dragana Laketic, Gunnar Tufte, Pauline Catriona Haddow, Norwegian University of Science and Technology	
19:00 - 23:00	<p align="center"><b>Conference Dinner and Prize Awards</b> Butterfly Restaurant Pier 33 on 1500 The embarcadero, San Francisco, CA 94133; Tel: (415) 864-8999; <a href="http://www.butterflysf.com">http://www.butterflysf.com</a></p>		

**SATURDAY, AUGUST 1, 2009**

TRACK I Room 304		TRACK II Room 305	
09:00 – 09:45	<p align="center"><b>Invited Keynote Address (Room 304): Adaptive Learning with New Pattern Recognition Method CHLAC</b></p> <p align="center">Tetsuya Higuchi National Institute of Advanced Industrial Science and Technology, Japan</p> <p align="center">Chair: Didier Keymeulen, Jet Propulsion Laboratory (JPL), USA</p>		
<p align="center"><b>BREAK 1</b> Room 307</p>			
10:15 – 11:45	<p align="center"><b>Panel (Room 304): Future directions in hardware/system design: can adaptivity help?</b></p> <p align="center">Moderator: Tughrul Arslan, The University of Edinburgh, UK</p>		
<p align="center"><b>BREAK 2</b> Room 307</p>			
<p align="center"><b>Session 1G: Reconfigurable Computing incl. Multi-Core Architectures</b></p> <p align="center">Chair: Karel Walters University of Twente, The Netherlands</p>		<p align="center"><b>Session 2H: Automated Design Methodologies and Tools (cont.)</b></p> <p align="center">Chair: Lukas Sekanina Brno University of Technology, Czech Republic</p>	
12:10 – 12:35	<p><b>Self-Scaling Stream Processing: a Bio-Inspired Approach to Resource Allocation Through Dynamic Task Replication</b> Pierre-André Mury, <i>Ecole Polytechnique Fédérale de Lausanne (EPFL)</i> Gianluca Tempesti, <i>University of York</i></p>	<p><b>Nominal-Yield-Area Tradeoff in Automatic Synthesis of Analog Circuits: A Genetic Programming Approach using Immune-Inspired Operators</b> Piero Conca, Giuseppe Nicosia, Giovanni Stracquadanio, <i>University of Catania</i> Jon Timmis, <i>University of York</i></p>	
12:35 – 13:00	<p><b>An FPGA-Based Web Server for High Performance Biological Sequence Alignment</b> Ying Liu, Khaled Benkrid, AbdSamad Benkrid, Server Kasap, <i>University of Edinburgh</i></p>	<p><b>A Bio-Inspired Agent Framework for Hardware Accelerated Distributed Pervasive Applications</b> Olivier Brousse, Jeremie Guillot, Gilles Sassatelli, Thierry Gil, Michel Robert, <i>Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier - LIRMM</i></p>	
<p align="center"><b>LUNCH</b> (on your own)</p>			
<p align="center"><b>Session 1G: Reconfigurable Computing incl. Multi-Core Architectures (cont.)</b></p> <p align="center">Chair: Karel Walters University of Twente, The Netherlands</p>		<p align="center"><b>Session 2H: Automated Design Methodologies and Tools (cont.)</b></p> <p align="center">Chair: Lukas Sekanina Brno University of Technology, Czech Republic</p>	
14:00 – 14:25	<p><b>Rapid Prototyping of an Improved Cholesky Decomposition Based MIMO Detector on FPGAs</b> Xuezheng Chu, Khaled Benkrid, <i>Queen's University Belfast</i> John Thompson, <i>University of Edinburgh</i></p>	<p><b>Comparison of the Uniform and Non-Uniform Cellular Automata-Based Approach to the Development of Combinational Circuits</b> Michal Bidlo, Zdenek Vasicek, <i>Faculty of Information Technology, Brno University of Technology</i></p>	
14:25 - 14:50	<p><b>Strategies in SIMD Computing for Complex Neural Bioinspired Applications</b> Jordi Madrenas, J. Manuel Moreno, <i>Technical university of Catalunya (UPC)</i></p>	<p>Please go to Session 1G in Track I</p>	
14:50 - 15:15	<p><b>Adaptive hardware real-time task scheduler of multi-core ATPA environment</b> Mi Zhou, Li-Hong Shang, Jiong-Zhang, Hui-Hua Jin, <i>Beihang University</i></p>	<p>Please go to Session 1G in Track I</p>	
15:15 – 15:45	<p align="center"><b>Concluding Remarks</b> Room 304</p>		

# ESPLANADE LEVEL



Start **Moscone Convention Center**  
747 Howard St  
San Francisco, CA 94103  
(702) 943-6059

End **Butterfly embarcadero**  
1500 The embarcadero  
San Francisco, CA 94133  
(415) 864-8999

When 7/31/09 after 6:00pm  
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Duration 25 mins in transit, 8 mins walking to/from  
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Begin by walking

Go to **Market St & 4th St** (takes about 6 mins)

Light rail - F - Market & Wharves - Direction: Fisherman's Wharf  
Service run by San Francisco Municipal Transportation Agency

**6:07pm** Leave from **Market St & 4th St**

**6:24pm** Arrive at **The Embarcadero & Bay St**

Walk

Go to **1500 The embarcadero** (takes about 1 min)



These directions are for planning purposes only. You may find that construction projects, traffic, weather, or other events may cause conditions to differ from the map results, and you should plan your route accordingly. You must obey all signs or notices regarding your route.

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