Evolutionary Recovery from Radiation Induced Faults on Reconfigurable Devices

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Abstract—Radiation Hard technologies for electronics are the conventional approach for survivability in high radiation environments. This paper presents a novel approach based on Evolvable Hardware. The key idea is to reconfigure a programmable device, in-situ, to compensate, or bypass its degraded or damaged components. The paper demonstrates the approach using a JPL-developed reconfigurable device, a Field Programmable Transistor Array (FPTA), which shows recovery from radiation damage when reconfigured under the control of Evolutionary Algorithms. Experiments with total radiation dose up to 350kRad show that while the functionality of a variety of circuits, including a rectifier and a Digital to Analog Converter implemented on a FPTA-2 chip is degraded/lost at levels before 100kRad, the correct functionality can be recovered through the proposed evolutionary approach. The Evolutionary Algorithm controls the state of about 1,500 switches that determine configurations on the FTPA-2 programmable device. Evolution is able to use the resources of the reconfigurable cells, even radiation damaged components, to synthesize a new solution.

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1. INTRODUCTION

Long-life space missions and extreme environments have characteristics such as high radiation level (Europa Surface and Subsurface mission, 5 MRad), high temperature (Venus Surface Exploration and Sample Return mission, 460°C) and low temperature (Titan in-situ mission, -180°C). Such missions and environments have dictated the need for new electronics technologies.

Electrons and protons in space can cause permanent damage in electronic devices that can lead to operational failure. Particularly, Single Event Effects (SEE) are radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs. These events can be either transient and non-destructive (Single Event Upset) or hard and potentially destructive events (Single Event Latchup).

One technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on Insulator (SOI), which allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is high. In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high radiation environments.

A reconfigurable chip developed at JPL, the FPTA-2 chip, is used in the experiment described in this paper [20]. We submitted this chip to radiation using JPL facilities, applying a total dose ranging up from 10kRads up to 75kRads at a time and a cumulative dose up to 350kRads. These parts are not radiation hardened. When the chip was back from the radiation chamber, the permanent radiation induced faults (single event latch-up) caused a deterioration in the behavior of some circuits (D/As, filters, rectifiers) previously downloaded/programmed onto the chip. We show that the correct functionality of these circuits can be recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using

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a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered. Evolution is able to use the resources of the reconfigurable cells, even the radiation damaged components, to synthesize a new solution.

The results indicate that using Evolvable Hardware technology we can design and develop electronic components and systems that are inherently insensitive to radiation induced faults by using on-board evolution in hardware to achieve fault-tolerant and highly reliable systems. The long term results of the proposed research would allow electronics to adapt to an extreme environment and long mission duration.

A number of researchers in the literature have examined the effect of radiation on CMOS devices [1,2]. These could be classified into those researchers who studied the effect of radiation on various cells and macro-blocks fabricated in silicon [3-9] or those who considered the design of radiation hardened components and cell libraries [10-14]. Works on studying the impact of radiation have considered custom implementation and conventional digital FPGA platforms such as Xilinx [15-19]. These works have been focusing on studying both total dose radiation effects, where the effect is permanent, and Single Event Upsets (SEU)s, where individual bits in memory elements flip when exposed to certain quantity of radiation.

However, most of these researchers seem to have focused on technologies which are above 0.5 micron and hence the effects could not be generalized to devices implemented in the latest Deep Sub Micron (DSM) technologies, where leakage currents dominate. In addition, no research has been carried out on the development of custom reconfigurable architectures implemented at transistor level hence enabling the implementation of both analogue and digital circuits.

This paper presents a framework for the development of radiation tolerant mixed analogue and digital circuits on a DSM reconfigurable CMOS device. Experiments are carried out in which the device is subjected to various radiation dosages, using an X-ray based radiation source, and the performance of the device is tested by mapping a number of functional circuits. When the device fails any of the tests, an evolutionary algorithm is used to recover the functionality of the device where possible.

The rest of this paper is structured as follows: Section 2 describes the Field Programmable Transistor Array (FPTA) device architecture. Section 3 describes the procedure followed during radiation tests. Section 4 describes the overall system architecture which includes the data acquisition system. Section 5 provides an analysis of results obtained. Finally, the main conclusions of the work are listed in section 6.

2. FPTA ARCHITECTURE

The FPTA is an evolution-oriented reconfigurable architecture (EORA). Important characteristics needed by evolution-oriented devices are *total accessibility*, needed in order to provide evolutionary algorithms the flexibility of testing in hardware any chromosomal arrangements, some of which may be dangerous for existing commercial devices (may lead to internal bus allocation conflicts and burn the chip) and thus forbidden, *granularity at low level* (here transistor) allowing evolution to choose/construct the most suitable building block for certain system, and *transparency*, which enables users to have access to internal device information, etc.

The FPTA has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture is cellular, with each cell having a set of transistors, which can be interconnected by other "configuration transistors". For brevity, the "configuration transistors" are called switches. However, unlike conventional switches, these can be controlled for partial opening, with appropriate voltage control on the gates, thus allowing for transistor-resistor type topologies.

The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view

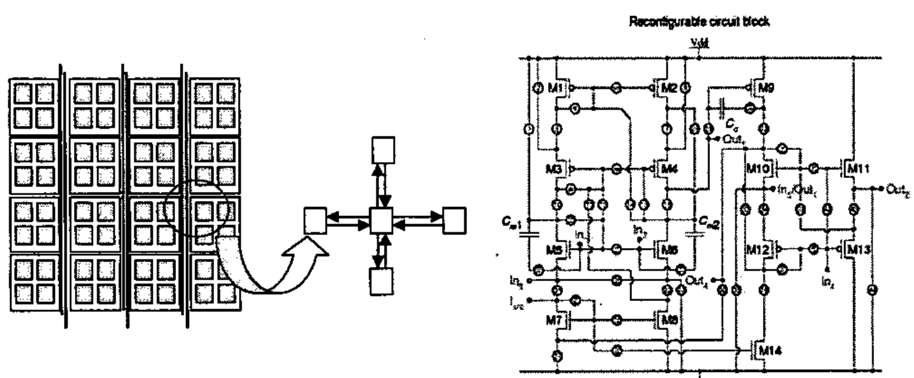


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors. This is the first mixed-signal programmable array, FPMA, in the sense that its cells can be configured as both analog and digital circuitry; with its 64 cells it can configure more Operational Amplifiers (OpAmps) than the largest commercial Field Programmable Analog Array (FPAA) chip (which contains only 20 OpAmps) [21].

3. Experimental Procedure

The radiation source used was an electron beams obtained from a dynamitron accelerator. The electrons are accelerated at an energy of 1 MeV in a small vacuum chamber with a beam of 8". The fluxes in the small chamber was 4.E9 [e/(s.cm2)] which is around 300 rad/sec.

The procedure for exposure to radiation, test, and recovery was as follows; 4 different samples of the FPTA chip were exposed to radiation at a time. Two of the samples were under electronic bias (chip B1 and chip B2), whereas, the other two remained un-biased (chip U1 and chip U2). Due to space limitations in the chamber, only two chips could be radiated at a given time, so the biased and un-biased sets were alternated under the same radiation dose.

Both the biased and un-biased sets were exposed to radiation doses ranging from 0 to 350Krad at 50Krad steps. Figure 2 illustrates the incremental radiation profile to which the chips were subjected to over a period of 7 days.

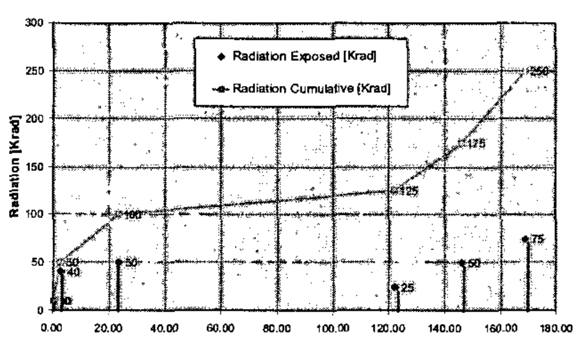


Figure 2: Cumulative radiation and experimental schedule.

After each radiation step both biased and un-biased sets were tested by downloading the configuration for the following tests/circuits respectively: Identity test, rectifier circuit, Tunable filter and 4-bit D/A converter circuit.

The identity test is specially designed to test the switching elements, i.e. transmission gates, within the FPTA. It operates by propagating a sinusoidal signal to the output through exercising the correct set of transmission gates within the FPTA. The rectifier, tunable filter, and the 4-bit D/A converter are examples of relatively large macro blocks of the FPTA which are utilized within sensor interfacing circuitry.

4. System Architecture

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm, as shown in Figure 3. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature and radiation experiments The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 to 200 generations require only 20 seconds.

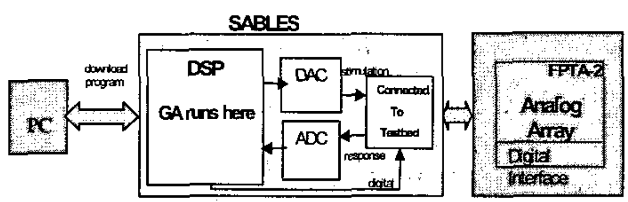


Figure 3: Complete System Architecture.

5. Results

Tables 1-4 illustrate results of radiation tests for dosages of 100Krad, 175Krad, 250Krad, and 350Krad respectively. Each table illustrates the experimental results with the various tests described in section 3 using both biased and un-biased test chip samples. The X symbol indicates the failure of the specific test with the corresponding chip, whereas V indicates its success. The elliptical shapes highlight a successful recovery through evolution. On the other hand a triangular shape indicates that the recovery was unable to obtain an acceptable output for the particular test. For each test any noticeable change in the behavior of input/output signals are reported. For example in table 1, U2 sample initially suffers a 50% drop in amplitude after reaching an accumulative dosage of 100krad (Half-wave rectifier). This is later recovered through evolution in 311 generations.

After a total dose of 100Krad a number of sample chips suffered from some distortion in the shape of the output waveform. This is mainly observed as a drop in amplitude of the signal. When evolutionary recovery is triggered most of these distortions are overcome and the true functionality is obtained. However, it must be noted in some cases that the fitness threshold in the evolutionary algorithm may require adjustment. This can be clearly seen when performing identity checks on the sample chip B2, where the fitness is adjusted from 4500 to 6000 (Table 1). Although the resulting sine wave has a slight clip on the rising edge, this is small enough not to distort the output waveform which is very similar to that applied on the input.

It could be noted form the table 1 that the un-biased chip U1 starts to malfunction at 100Krad with most tests failing drastically such that recovery is not possible.

Table 1: Experimental results at 100kRads on chip samples un-bias U1, U2 and bias B1 and B2.

	U1		U2		B1		B2	
	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution
IDENTITY	human		human		human		human	
test on cell0; cell16; cell17; cell5 switches: S2-S31-S24-S29-S30-S57-S71	X response flat	X response flat for all chromosomes	V		V		X shape output distorted	V recovered - raise fitness threshold to 6K from 4.5k - sine wave slightly clipped on the rising edge
test on cell0; cell16; cell17; cell5 switch: S2	X response flat	X response flat for all chromosomes	V		V		V	
	ANALOG							
HALF-WAY RECTIFIER	human		human		human		human	
4cells: cell0, cell1, cell2, cell3	X response flat	X response flat for all chromosomes	X amplitude drop 50%	V recovered generation=311 fitness=[illegible]	X amplitude drops 50%	V recovered generation=300 fitness=4500	X low amplitude sinwave	V recovered generation=242 fitness=4898
TUNABLE FILTER								
10 cells: cell0 to cell9 frequency: amplify 1kHz and attenuate 10kHz input:			V INPUT: for input 1kHz+10kHz 1kHz = -11.76dB 10kHz= -19.81dB OUTPUT: 1kHz= -12.54dB 10kHz= -31.27dB		V INPUT: for input 1kHz+10kHz 1kHz = -11.26dB 10kHz= -18.58dB OUTPUT: 1kHz = -11.43dB 10kHz = -30.49dB			V recovered but shape distorted with harmonics around 10kHz INPUT: for input 1kHz+10kHz 1kHz = -11.31dB 10kHz= -19.05dB OUTPUT: 1kHz = -9.41dB 10kHz = -33.67dB
4bits DAC								
20cells: cell0 to cell19	X O4= signal bit4	X fitness=13 generation=200 not achieving bit2, bit3 and bit4	V		V		X bit1: is working bit4: modification of level in output value	V recovered fitness=4.0 generation=200 amplitude drops by 20%

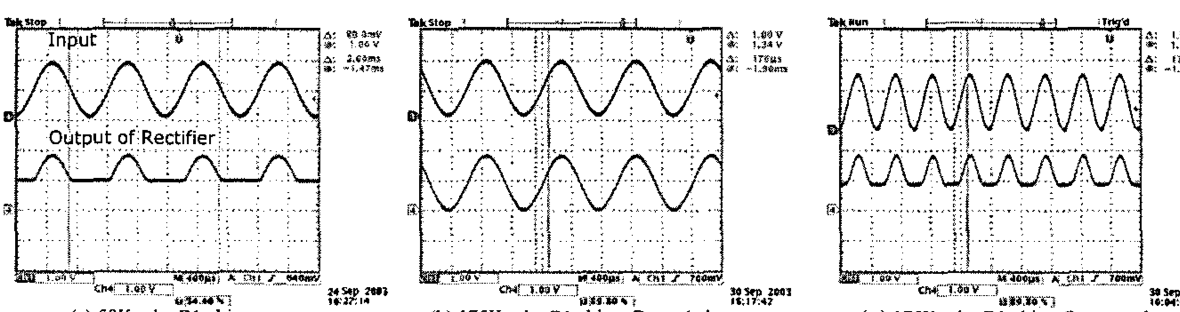
Table 2: Experimental results at 175 kRads.

	U1		U2		B1		B2		REFERENCE CHIP
	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human
					ADDRESS DECODER & FLIP-FLOP				
IDENTITY	human		human		human		human		
test on cell0, cell1, cell2, cell3 switches: S2-S31-S24-S29-S30-S57-S71	V		V		V		V		
					ANALOG				
HALF-WAY RECTIFIER	human		human		human		human		
4cells: cell0, cell1, cell2, cell3	X -The shape has been changed. No rectification.	V -301 generations -fitness 4272	V		X -The input is observed at the output	V -677 generations -fitness 7906	X -The input waform is observed at the output.	V -200 generations -fitness 16217	
TUNABLE FILTER									
10 cells, cells0 to cells9 frequency: amplify 1kHz and attenuate 10kHz input:	V FREQUENCY ANALYSIS: (result of sweep ok: no harmonics) INPUT: for input 1kHz+10kHz 1kHz = -12.64 dB 10kHz= -19.96 dB OUTPUT: 1kHz = -14.51 dB 10kHz = -36.99 dB		V FREQUENCY ANALYSIS: (result of sweep ok: no harmonics) INPUT: for input 1kHz+10kHz 1kHz = -12.63 dB 10kHz= -19.97 dB OUTPUT: 1kHz = -15.61 dB 10kHz = -37.72 dB		V INPUT: for input 1kHz+10kHz 1kHz = -12.62 dB 10kHz= -20.01 dB OUTPUT: 1kHz = -14.46 dB 10kHz = -35.34 dB Time response distorted slightly harmonics exist around 1K and 10K		X INPUT: for input 1kHz+10kHz 1kHz = -12.64 dB 10kHz= -20.00 dB OUTPUT: 1kHz = -21.87 dB 10kHz = -45.24 dB low amplitude at output	V INPUT: for input 1kHz+10kHz 1kHz = -12.70 dB 10kHz= -19.27 dB OUTPUT: 1kHz = -13.74 dB 10kHz = -30.38 dB	Reference Chip INPUT: for input 1kHz+10kHz 1kHz = -11.33dB 10kHz= -19.05dB OUTPUT: 1kHz = -12.21dB 10kHz = -30.89dB
4bits DAC									
20cells: cell0 to cell19	X -big bit four Jump and slight bit three jump (discontinuity).	X recovered a 3bits DAC	V		X similar to U1, with more jump on B4	V -low voltage range -small glitch for bit4 -fitness=6.0	X -bit 4 same as U1 -bit 1 has a slight jump.	V -low voltage rate -fitness=6.5	Reference Chip fitness=4.1

As the radiation dosage is increased to 175 Krad, the distortion on the output increases. For example, the rectifier for both B1 and B2 passes the input unchanged. However, in almost all cases the evolutionary recovery system is able to correct the output to the required shape. Figure 4(a) illustrates the response of the rectifier at 50krad on the sample B1 chip. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input shown on Figure 4(b). When the evolutionary mechanism is activated, the correct output response is retained as shown in Figure 4(c).

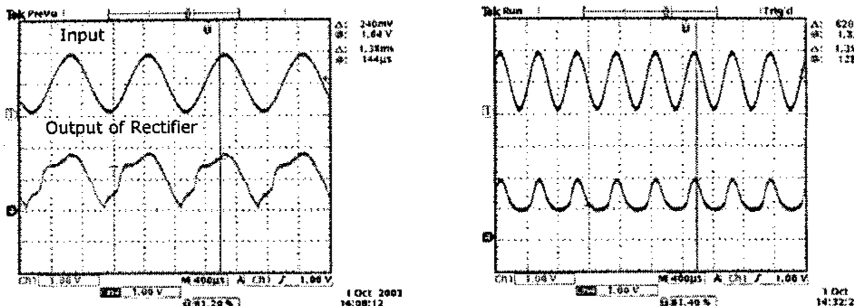
As the dosage is increased to 250Krad (Table 3), cases appear where the evolutionary algorithm is unable to recover the correct functionality on the output (discarding U1 due to its inconsistent behavior). However, in most cases recovery is achieved. Again considering the rectifier circuit at 250krad as illustrated in Figure 5(a), the output response is clearly distorted due to radiation. However, the correct output response is recovered once the evolutionary mechanism takes over, even though the final circuit suffers from some non-ideal behavior when the output is low.

As the dosage reaches 350 Krad (Table 4), there is a clear failure pattern with all tests, with the evolutionary algorithm unable to recover any of the required functionality.



(a) 50Krad – B1 chip (b) 175Krad – B1 chip – Degraded (c) 175Krad – B1 chip - Recovered

Figure 4: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.



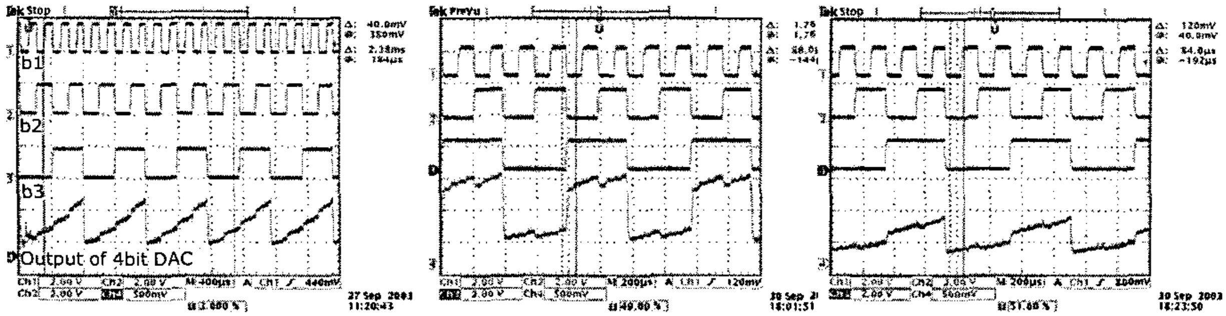
(a) 250Krad – B1 chip - degraded (b) 250Krad – B1 chip - recovered

Figure 5: Response of the Rectifier circuit at (a) 250kRads resulting in distortion, followed by (b) recovery through Evolution

Table 3: Results with 250kRads

	U1		U2		B1		B2		REFERENCE CHIP
	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human
	ADDRESS DECODER & FLIP-FLOP								
IDENTITY	human		human		human		human		
test on cell0; cell1; cell2; cell3 switches: S2-S31-S24-S29-S30-S57-S71	X -output 0 -this is tue for cells 47,48,0,1,32 -also true with s2 closed while input on	X nearly a flat input, however, there is the trace of input following the output	V		X -slight deterioration in output. Sine wave slightly dented on both sides. This is tue for cells 16 also true with s2 closed while input on in2 and output in1	V -slight decrease in voltage level -sine wave clipped on left and right hand sides.	X -output 0 This is tue for cells 1,4,5,16,17 also true with s2 closed while input on in2 and output in1	V -perfect waveform obtained	
	ANALOG								
HALF-WAY RECTIFIER	human		human		human		human		
4cells: cell0, cell1, cell2, cell3	X -output flat	X -Evolution is not even close to the solution.	V		X -Output follows the input as a sine wave, with large distortion on the right hand side.	V -The bottom is not perfectly flat. -fitness is 7306. -after 1337 generations.	X -output follows the input with slight reduction in amplitude.	V -perfect recovery. Fitness:4279 after 79 generations. -In a number of runs the GA was not able to spot perfect solutions even though these were spotted on the scope. Either the fitness function is not sound or the sampling may be causing errors.	
TUNABLE FILTER									
10 cells: cells0 to cells9 frequency: amplify 1kHz and attenuate 10kHz input:	X output flat INPUT: for input 1kHz+10kHz 1kHz = -12.59 dB 10kHz= -20.00 dB OUTPUT: 1kHz = -37.02 dB 10kHz = -44.37 dB	X -no response to evolution.	V FREQUENCY ANALYSIS: result of sweep: no harmonics) INPUT: for input 1kHz+10kHz 1kHz = -12.59 dB 10kHz= -19.96 dB OUTPUT: 1kHz = -15.54 dB 10kHz = -37.46 dB		X output flat FREQUENCY ANALYSIS: INPUT: for input 1kHz+10kHz 1kHz = -12.58 dB 10kHz= -19.96 dB OUTPUT: 1kHz = -42.03 dB 10kHz = -47.07 dB	X -best response similar to input, with loss of sine shape and lowering of level.	X -output has v. low amplitude. INPUT: for input 1kHz+10kHz harmonics around 10K and 1K 1kHz = -12.57 dB 10kHz= -19.94 dB OUTPUT: 1kHz = -22.74 dB 10kHz = -45.20 dB	V FREQUENCY ANALYSIS: result of sweep: low harmonics around 10KHz) INPUT: for input 1kHz+10kHz 1kHz = -12.70 dB 10kHz= -19.24 dB OUTPUT: 1kHz = -16.54 dB 10kHz = -37.76 dB a number of runs faoled producing: --best response similar to input, with loss of	
4bits DAC									
20cells: cell0 to cell19	X -output follows bit4	X -sometimes the output is the same as bit number 4 (with a small square wave on high levels) and sometimes output flat.	V		X -output follows bit 4, with some sort of DAC behaviour at low and high levels	V?? -a monotonic wave was obtained similar to the DAC, however the amplitude is dropped by half and levels are not clear. Fitness 9.5.	X -The output looks like a dac but the shape is not monotonic, has ups and downs, and some sudden jumps. Better than u1 and b1 though.	X	

Figure 6 demonstrates another example of recovery through evolution using the example of the 4-bit DAC circuit. Figure 6(a) illustrates a correct functioning DAC at 100Krad. When radiation dosage is increased to 175Krad, the circuit malfunctions with clear loss in discrimination between various input values. This is associated with a loss in the monotonic nature of the response, see Figure 6(b). When evolution is activated the response is recovered, however, as could be seen from Figure 6(c) there is some deterioration in the signal level.



(a) 100Krad – B1 chip (b) 175Krad – B1 chip - degraded (c) 175Krad – B1 chip - recovered

Figure 6: Response of a 4bit DAC circuit (least significant bit b_0 is not shown) at (a) 100kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of "monotonicity", followed by (c) recovery through Evolution at 175kRads.

Table 4: Results with 350kRads.

	U1		U2		U2		B1		B2		REFERENCE CHIP
	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human	Recovering Circuit by Evolution	Reference Circuit obtained by Evolution or by Human
	ADDRESS DECODER & FLIP-FLOP										
IDENTITY	human		human				human		human		
test on cell0; cell1; cell2; cell3 switches: S2-S31-S24-S29-S30-S57-S71			X cells 9,22,25,33,38,49,51,6 work. The rest of the cells did not work.	Recovered using cell 0,1	OK		X cell0, flat at 0, cell1:flat at 1v, cell 2: flat at 1v, cell 23: flat at 0, cell 24: flat at 0, cell 64: a rectifier like signal with .6V amplitude		X cell0, flat at 0, cell1:flat at 0v, cell 23: flat at 0, cell 24flat at 0, cell 64,63: 0		
S2: test on cell 0,1,4,5,16,17,20,21			OK		OK		X cell0, rectifier like output with 0.4V amplitude, cell1: flat at 0.4v, cell4: same as cell0, cell5: flat, cell16: input distorted and output flat, cell17: as for 16, cell20: a sine wave output with 0.4 amplitude, cell 21: flat.		X cell0, rectifier like output with 0.4V amplitude, cell1: flat at 0.4v, cell16: same as cell0, cell17: as for cell 0.		
CONTROL CELL TEST	human		human				human		human		
Cell Test Qz0 (output of a flip-flop of test cell) [pin 168] output pin Sel_c0_test (select of the flip-flop of the test cell - issue by address decoder) [pin 162] D0 [pin 66]: input of flip-flop input pin Sel_wr_test [pin163] input pin Clr_test [pin 164]							X		V		
	ANALOG										
HALF-WAY RECTIFIER	human		human				human		human		
4cells: cell0, cell1, cell2, cell3			X output follows the input with very low amplitude	recovered after 149 generations with the fitness score of 4104							
TUNABLE FILTER											
10 cells: cells0 to cells9 frequency: amplify 1kHz and attenuate 10kHz input:			OK								
4bits DAC											
20cells: cell0 to cell19											

6. CONCLUSIONS

The paper has presented a mechanism for adapting a mixed analogue reconfigurable platform under total dose radiation faults. Experiments were carried out which exercised the reconfigurable device up to 350Krad radiation dosages demonstrating that the technique is able to recover functionality of blocks such as analogue to digital converters up to 250Krad radiation dosage.

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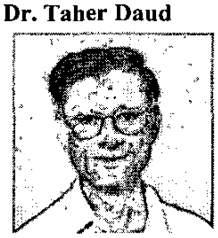

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