A Multi-objective Genetic Algorithm for On-chip Real-time Optimisation of Word Length and Power Consumption in a Pipelined FFT Processor targeting a MC-CDMA Receiver

Nasri Sulaiman[1] and Tughrul Arslan[1,2]

[1] School of Engineering and Electronics
The University of Edinburgh, King's Buildings
Mayfield Road, Rdinburgh, EH9, 3JL, UK
[2]Institute for System Level Integration
The Alba Centre, Alba Campus
Livingston, EH54 7EG, UK.
N.Sulaiman@ed.ac.uk, T.Arslan@ee.ed.ac.uk.

Abstract

This paper presents a multi-objective Genetic Algorithm for on-chip real-time optimisation of word length and power consumption in a fixed-point pipelined Fast Fourier Transform (FFT) processor targeting on MC-CDMA receiver. The multi-objective GA is used to find solutions for the FFT coefficients which have optimum performance in term of signal to noise ratio (SNR) and power consumption. The results demonstrate that the GA can find solutions which are optimised for both objectives. Results also show that there is a significant reduction in power consumption while maintaining the SNR after the optimisation. Optimisation from 16-bit to 11-bit, results in power reduction of 6.6% and an average error of 0.69 dB.

1. Introduction

Power consumption is an important parameter in realiasing VLSI systems for portable wireless telecommunications like multi-carrier code division multiple access (MC-CDMA) due to battery lifetime [1]. An FFT processor is the main component in the MC-CDMA receiver which contributes the most power consumption [2]. Power consumption of FFT processor depends on the size of the word length of the data and the FFT coefficients [3]. Larger word length means higher SNR for a fixed-point FFT. Since the errors in FFT depend on the SNR, where the higher the SNR the lower the errors, it is important for the FFT processor to have larger word length. However, power consumption will be increased due to more switching activities [4]. It is therefore highly desirable to design an FFT processor which has a good trade-off between power and SNR. This is a complex, multi-objective task which requires simultaneous optimisation of competing parameters such as power and SNR. It requires parameter prioritisation which may reduce the overall quality of solution since it is difficult to combine all the objectives into a single cost function [5].

Multi-objective GAs have been applied in some areas of digital VLSI design, for examples [6], [7], [8] and [9]. The work in [6] is a structural synthesis of VLSI circuits where the GA is used to find designs which satisfy the functionality constraints and the hardware-specific criteria such as area and delay. In [7], the GA is used to optimise CMOS based DSP systems under multiple design constraints such as power, speed and area. The work in [8] describes a CAD tool which selects low-voltage components for complex SOC system implementation where the individual components are optimised in terms of minimum area and power consumption while maintaining the area, power and supply voltage constraints of the system. The researches in [9] use a GA to generate an optimised finite impulse response (FIR) design in terms of area and latency.

This paper describes the analysis of the impact of a multi-objective GA for word length optimisation of fixed-point FFT coefficients on power consumption. The work investigates the possibility to find a solution for the FFT coefficients which have optimum performance in terms of SNR and power consumption. This is a critical design issue for future wireless receivers which combine high performance and low power. A specific issue of concern in this research would be targeting the multi-objective process for on-chip optimisation of a complete wireless MC-CDMA receiver [2].

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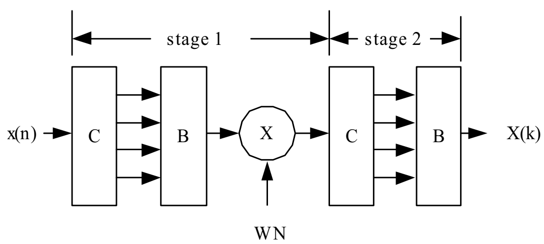
2. FFT Design

The FFT used in this work is based on the radix-4 single-path delay commutator (R4SDC) architecture proposed by the authors in [10]. This architecture is chosen because it has been used recently in building the largest ever single chip pipelined FFT processor for HDTV application [11] and has tremendous saving in hardware and power consumption for real-time applications [12]. Figure 1 shows the block diagram of a 16-point FFT based on this architecture. Figure 2 displays the corresponding flow graph where each open circle represents the summation while the dots define the stage boundaries. The number inside the open circle is the value of m_1 (stage 1) or m_2 (stage 2). The number outside the open circle is the FFT coefficients applied.



C = Commutator, B = Butterfly

Figure 1: Block diagram of a 16-point R4SDC pipelined FFT

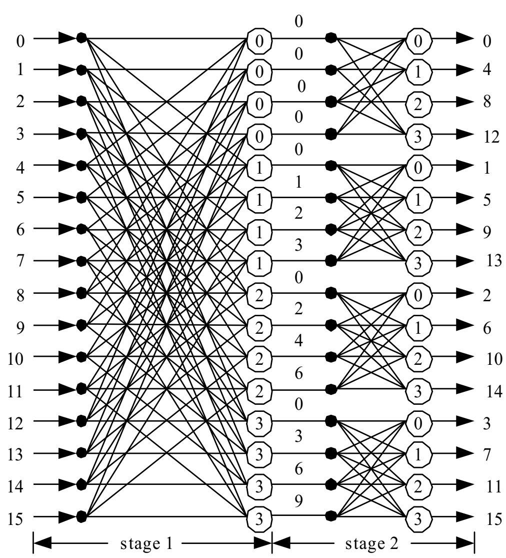


Figure 2: Signal flow graph of a radix-4 16-point FFT

3. Genetic Algorithm (GA)

An Evolvable Hardware (EHW) uses an evolution algorithm (EA) such as genetic algorithm (GA) [13], genetic programming (GP) [14], evolutionary programming (EP) [15] and evolutionary strategies (ES) [15] as its main adaptive mechanism. However, GA is the most dominant approach in EHW because it has emerged as a powerful approach to solving more difficult optimisation problems [16]. Some examples of EHW which use GA in their applications are the work done by the authors in [16], [17], [18] and [19]. Their work is classified as single-objective GA where a single fitness measure is optimised. However, many real world problems may have multiple conflicting objectives which requires multi-objective GA to optimise multiple fitness measures [20].

3.1 Objectives

The GA is used to optimise the word length of the fixed-point FFT coefficients for two objectives:

(1) the coefficients should maintain the desired SNR i.e., have smallest total error as possible and,

(2) they should have the lowest power consumption. These two objectives conflicts with each other, as an increase in the word length will reduce the error (maintains the SNR) but increases the power consumption. Fitness evaluations for the SNR and power consumptions are explained in details in sections 3.4 and 3.5 respectively.

3.2 Chromosome

The chromosome representation for the FFT coefficients is shown in Figure 3. In this representation, each stage contains 2 fields of information: coefficients and control. The coefficients field contains the real and imaginary parts of the FFT coefficients and data coefficients for every stage except in final stage which contains only the data coefficients. The control field contains control bits and is used to select either coefficient optimisation or data optimisation or both of these.

The size of the chromosome depends on the size of the FFT. For a 16-point FFT, the number of stage is 2. The first stage consists of 16 FFT coefficients and 16 data coefficients. The second stage only consists of 16 data coefficients. The initial coefficients are obtained from the MATLAB FFT procedure and are represented as 16-bit numbers. A population size of 50 is chosen through experimentation as it provides sufficient solution diversity.

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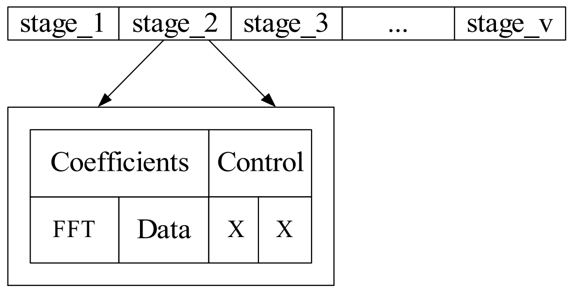

Figure 3: Chromosome structure

3.3 Genetic Operators

The genetic operators used in this work are extracted from standard GA procedure which includes selection using roulette wheel, crossovers and mutation [13]. In this work, the rates for crossovers and mutation are chosen as 90% and 10% respectively. This was chosen through experimentation as it provides sufficient solution diversity.

3.4 SNR Fitness Evaluation

Every solution obtained by the GA will be first evaluated for the SNR fitness. The SNR fitness is evaluated in 3 steps of calculation. The first step is to determine the FFT outputs for each solution. In the second step, the corresponding SNR values for all the FFT outputs are calculated using the formula in (1).

$$SNR = 10\log_{10}\left[\frac{(R_{16})^2 + (I_{16})^2}{(R_{16} - R_{wl})^2 + (I_{16} - I_{wl})^2}\right] \quad (1)$$

where R_{16}, I_{16}, R_{wl} and I_{wl} are the real and imaginary parts of the FFT output before and after optimisation respectively.

Finally, the SNR value for each FFT output will be compared with the targeted SNR value. If the former is lower than the latter, the total error will be calculated as the sum of all the differences between the latter and the former. This will represent the score of the SNR fitness. The higher the score, the closer is the SNR of the solution to the desired SNR.

A solution which has a total error less than the maximum error allowed is considered as an acceptable solution. The GA will continue to search for an acceptable solution until a maximum number is reached. In this work, the values of targeted SNR, maximum error allowed and maximum number of acceptable solution are chosen as 60 dB, 20dB and 20 respectively. In practice, these figures may change in real-time depending on the environment in which an MC-CDMA receiver is situated, which will in turn affect channel requirements like delay spread, SNR, bandwidth and bit error rate.

3.5 Power Fitness Evaluation

Power analysis is performed for the every acceptable solution obtained from the SNR fitness evaluation. The objective for this analysis is to evaluate the power consumption and associate this figure with the figure obtained from the SNR fitness. This task is accomplished by synthesising the verilog code of FFT hardware, parasitic back-annotation, followed by power evaluation. The figures regarding the total error and related power consumption for an individual solution will be stored in a lookup-table. The lookup table contains the following information for a particular solution.

(1) Word length: The specified word length.
(2). SNRT : The minimum SNR required.
(3) Error : The total error.
(4) Power : Pre analysed power consumption.
(5) Coefficients : The FFT and data coefficients.

3.6 Overall Fitness Evaluation

The overall fitness is evaluated as a weighted sum of the SNR and power fitness and defined as below in (2).

$$\text{Overall\_fitness} = \alpha.\text{SNR\_fitness} + \beta.\text{Power\_fitness} \quad (2)$$

where α and β are the respective weights.

A solution with lower overall fitness will have higher SNR and lower power and vice versa. In this work, the maximum overall fitness is set to 140. This figure is obtained by summing the maximum figures for the total error and power consumption which are 20 and 120 respectively. The best performance of the GA in obtaining the solutions can be determined by varying the values of any of the weight parameters, α and β. Here, the value of α is varied from 1 to 10.

4. Results

Figure 4 shows the GA search results of the FFT optimisation for different word lengths ranging from 15-bit down to 11-bit. The results provide 3 important pieces of information. The first is about the smallest total error obtained in optimisation for a particular word length. For example, the smallest total error for 15-bit, 13-bit and 11-bit word lengths are 0 dB, 4 dB, and 11 dB respectively. This clearly shows that the total error reduces as the word length increases. This also implies that the optimisation of word length from 16-bit to 11-bit for a 16-point FFT, is associated with an average error of about 0.69 dB. This figure shows a good indication that the solution obtained has a close SNR figure with the targeted value.

The second piece of information highlights when the first best acceptable solution is found. For instance, the first

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acceptable solutions for 11-bit and 12-bit optimisations are found in generations 6 and 4 respectively. The results also show that the GA search is able to find acceptable solutions with several different values of total error, for example, the total error in 6 and 9 generations for 11-bit word length are 16 dB and 9 dB respectively. This is another advantage of our GA.

The third piece of information is about the convergence of the solutions. From Figure 4, it is clearly shown that the solutions for all the optimisations converges to a value below the maximum total error allowed after a few generations. This implies that the GA is capable to provide promising solutions for the optimisation problem.

The optimisations are continued under the same conditions for word lengths lower than 11-bit such as 10-bit, 9-bit, 8-bit and 7-bit. However, the smallest total errors obtained are 30 dB, 126 dB, 187 dB and 309 dB which are found for the first time in generations 176, 12, 405 and 19 respectively. The total errors obtained stay fixed at these points in the following generations and never go below the maximum total error allowed even after 5,000 generations.

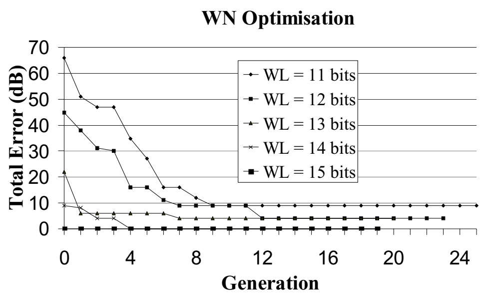

Figure 4: GA search results for SNR fitness

Figure 5 displays the power consumption for the best solutions shown in Figure 4. The figure clearly shows that as the word length increases from 11-bit to 15-bit, the total errors decreases from 10 dB to 0 dB. On the other hand, the power consumption increases from 114 mW to 119 mW. In the case of 11-bit optimisation, the power consumption is 114 mW as compared to the 122 mW when the word length is 16-bit. There is about 6.6% reduction in power consumption. This shows that there is a potential of more power consumption reduction which can be achieved as the GA optimises the word length at some other parts of the FFT.

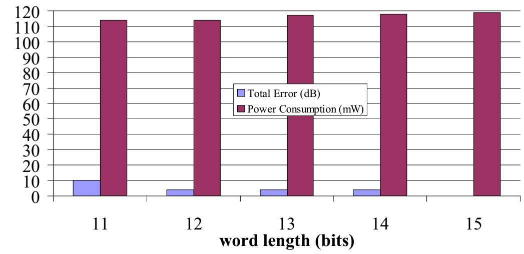

Figure 5: Total Error vs Power Consumption

Figure 6 depicts the results of the optimisation further down to 7-bit. The power consumption for the 7-bit word length is 111 mW. This shows that there is a further power reduction as the word length is decreased further. However, the total error is also increases beyond the maximum total error allowed.

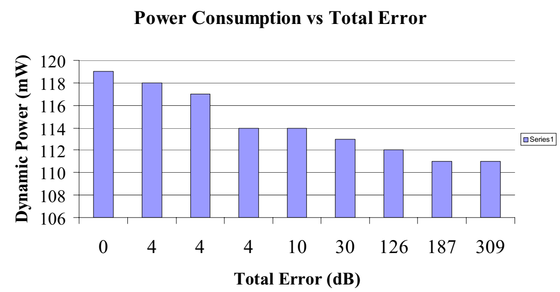

Figure 6: Power Consumption vs Total Error for 15-bit down to 7-bit optimisation

Figure 7 shows the best performance of the multi-objective optimisation where the values of α and β are found to be 1 and 1 respectively. The results show that for the cases of 15-bit and 14-bit optimisations, the GA can find a solution with the fitness value of 120 and 119 respectively. These values are very close to the sum of the minimum total error and minimum power consumption. This means that the solutions are optimised for both objectives. The solutions for the other 3 cases have fitness values less than the sum of the maximum for both total error and power consumption. This implies that they are optimised for at least one objective. Table 1 displays the times taken by the GA to find the solutions for optimisations from 15 bits to 11 bits. The results reflect the average time obtained from 10 runs running at the Sun Blade -100 workstation. It is clearly shown that as the word length decreases, the time taken increases as the level of optimisation becomes more difficult.

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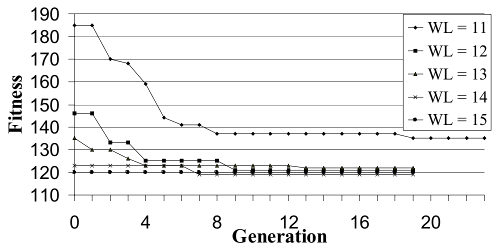

Figure 7: Best multi-objective GA performance search result

Table 1: GA execution time

	Word length	time
1	15 bits	1.2s
2	14 bits	1.3s
3	13 bits	1.3s
4	12 bits	1.7s
5	11 bits	2.3s

Figure 8 illustrates the performance of the multi-objective optimisation where the values of α and β are 3 and 1 respectively. The results show that solutions for the case of 15-bit and 14-bit optimisations are still optimised for both objectives. The GA also found solutions which are at least optimised for one objective for the other cases but it took longer time.

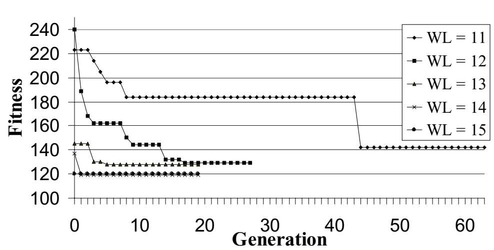

Figure 8: Average multi-objective GA performance search result

5. Conclusion

In this paper we have described a multi-objective Genetic Algorithm for on-chip real-time optimisation of word length and power consumption in a fixed-point pipelined Fast Fourier Transform (FFT) processor targeting on MC-CDMA receiver. Results show that there is a significant reduction in power consumption while maintaining the SNR after the optimisation. Optimisation from 16-bit to 11-bit, results in power reduction of 6.6% and an average error of 0.69 dB. The results also show that the GA is able to find solutions which are optimised for both objectives.

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