

Custom Reconfigurable Architecture for Autonomous Fault-Recovery of MEMS Vibratory Sensor Electronics

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Abstract

This paper presents a novel custom-reconfigurable architecture, which is tailored to accomplish the electronic circuits associated with MEMS vibratory sensors. The paradigm of this research work focuses on the JPL/Boeing gyroscope. Since the type of the sensor is vibratory, its dynamics are sensitive to temperature variation. In addition to this, the electronics associated with it, must be tolerable to operational deviations due to radiation. Therefore, our scope is to embed the two compensation loops of the gyro within an efficient adaptive platform able to compensate for the high range of gyro's dynamics and radiation tolerance zone. In this paper we demonstrate the capability of our architecture to cope with permanent faults, which occur on the gyro electronics.

1. Introduction

The design of integrated VLSI systems, which are able to cope with unanticipated faults, finds extensive use in aerospace and safety-critical applications. These faults can either be caused due to fabrication imperfections or random defects produced by harsh environments. A fault-tolerant system must have the capability to maintain its performance within acceptable operational margins in the presence of numerous hardware failures. Particularly, in highly radiated environments, the existence of alpha-particle and cosmic-ray radiation creates single-event-upset (SEU) errors. These errors mainly affect the latch state and the memory cells of the electronic devices. Custom-reconfigurable architectures (RAs) present the most adequate mean to provide fault-recovery solution, especially in applications in which hardware adaptability must accompany reduction of silicon-area

and power consumption. In addition to this, whenever human intervention is impossible, it is imperative for the system to get autonomously reconfigured in order to compensate to faults. Our previous research work [1] revealed that a specially tailored genetic algorithm (GA) is best suited for the reconfiguration of adaptive architectures. This paper presents a custom RA that suits the realization of the electronics associated with the JPL/Boeing gyroscope. JPL gyro is a vibratory MEMS sensor that presents lower mass and cost and higher reliability compared with conventional gyro sensors. However, as any other common vibratory sensor, it employs feedback compensation to achieve *harmonic excitation of selected modes, disturbance rejection and tuning* of the sensor's dynamics. These tasks are accomplished by two control loops named *drive loop* and *sense rebalance loop*. Moreover, there is also a *demodulation stage* that estimates the angular rotation rate of the gyro by demodulating the sense rebalance signal with respect to a measurement of the drive loop response [2]. This paper is mainly focused on the distinct implementation of the associated electronics that accomplish the feedback compensation and shows the efficiency of the architecture to cope with operational degradation due to faults.

2. Gyroscope electronics

Figure 1 demonstrates a high-level schematic [2] that illustrates the functionality of the integrated digital circuit, which accomplishes the control and signal processing tasks of the JPL/Boeing gyro. It can be seen that the drive loop is implemented with a non-linear *automatic gain controller* (AGC), which in-turn mainly consists of FIR 1, FIR 2 and a proportional-integral (PI) controller. In addition to this, the sense-rebalance loop is implemented with a linear filter FIR

3 and finally the demodulation stage consists of FIR 4, 5 and FIR 6, 7. For the scope of this paper, the capability of our architecture to tolerate with faults will be shown by implementing a lowpass (FIR 2) and passband (FIR3) filter that both meet the specification of the targeting application.

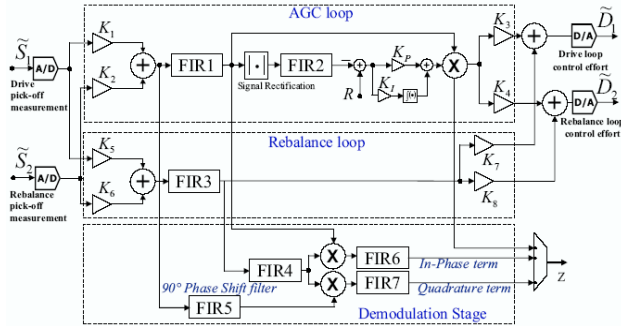


Figure 1. Gyro high-level schematic electronics

3. System architecture

Our proposed architecture combines both the adaptability of reconfigurable devices and the powerful search methods of GAs. This amalgam provides distinctive characteristics such as autonomous reconfiguration and recovery from faults. Compared with previous research achievements [3] on this field, this design presents several advantages. Firstly, it can evolve each part of the FIR filter (delays, arithmetic-unit and accumulation unit). Secondly, the circuit utilizes a mechanism to switch-off all the redundant hardware components. Figure 2 presents the overall system, which consists of the custom reconfigurable device that is adequate to realize high-order FIR filters and the GA that guides the reconfiguration process and provides the best possible configuration. The GA utilizes a radix-4, 256-point FFT since the evolution of the filters is performed in the frequency domain. This approach presents superiority over evolution in time domain [1] since the same frequency response can be achieved with different sets of coefficients. Moreover, for the evolution of the filters, random data samples are used because one of our purposes is to control and avoid overflow and saturation. Consequently, the output of the RA is obtained and then the frequency response of the input $X(z)$ and output $Y(z)$ is calculated in order to obtain the square magnitude of the system. Finally, the system uses an overflow prevention and saturation control mechanism, which is based on the adoption of a hybrid arithmetic representation, which employs both fixed-point and the simplest form of floating-point arithmetic. Based on this mechanism each configurable arithmetic/logic unit (CALU) uses an additional bit (protection-bit), which

indicates whether there is the presence of a binary exponent of three. Figure 3 shows an example in which the result of the addition will overflow. However, the system takes three actions to prevent it. Thus, if the protection-bit is logic 0, the adder uses internally an extra bit in order to correctly calculate the result. Subsequently, the data sample is shifted right by three and the protection-bit is latched to logic 1 to indicate that there is a binary exponent of 3.

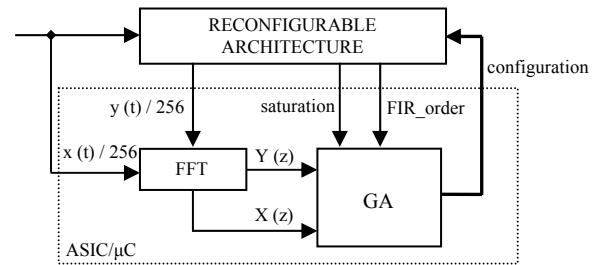


Figure 2. Overall architecture

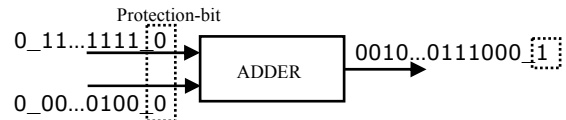


Figure 3. Overflow & saturation mechanism

3.1. Reconfigurable architecture

Figure 4 depicts how the programmable elements are interconnected, in order to provide an optimal physical mean for the design of digital filters. The RA is based on the POF technique [4], which is suitable for area and power optimization. Hence, the arithmetic-unit of the system consists of primitive operations such as adders/subtractors and right/left shifters (A/S and R/L-S CALUs). The circuitry between two subsequent A/S CALUs is called configurable arithmetic/logic block (CALB) and is illustrated in figure 4 within the dashed frame. Moreover, non-adjacent CALBs are connected to each other via 2:1 multiplexers, according to figure 5. This additional interconnection scheme is quite beneficial because it helps the system to control the order of the implemented filter and avoid faulty components by providing alternative routing solutions.

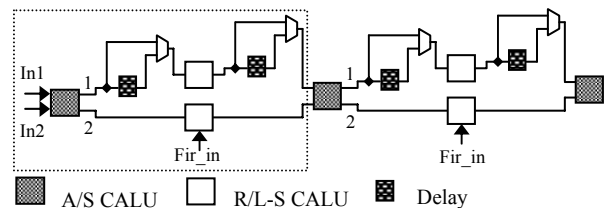


Figure 4. Reconfigurable structure

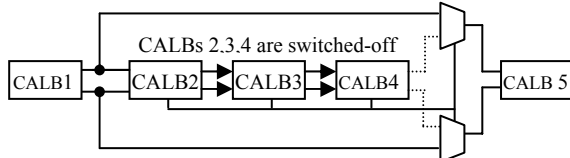


Figure 5. Power-consumption control mechanism

3.2. Genetic algorithm

The problem of identifying the binary configuration for the RA, based on a certain specification and the random appearance of faults, is uniquely suited to GAs. Each individual of the population encodes the control bits of the programmable elements. In figure 2 it can be seen that the GA considers the order of the evolved filter after each generation. This approach speeds-up significantly the convergence of the GA since it reduces the search space of the algorithm. Concerning the methodology ($\mu+\lambda$) of the GA, the initial population consists of 50 individuals, which after reproduction, is extended to 100. After evaluation and ranking the best chromosome is selected through elitism and in conjunction with another 49 chromosomes, which are selected through tournament selection, compose the new population. The fitness-function is given by the ratio between the evolved and the ideal squared magnitude [1].

$$Fitness = \sum_{i=0}^{127} (|F(j\omega)_{ideal_i}|^2 / |F(j\omega)_{evolved_i}|^2) - penalty_{sat_i} - penalty_{fir_order_i}$$

The ideal squared magnitude is pre-computed according to the targeted filter specification, while the evolved one is calculated by dividing the square of the output by the square of the input. Finally, the fitness includes another two objectives that are associated with the penalty, which is proportional to the occurrence of saturation events and the order of the evolved filter.

4. Simulation results

This section initially presents the results of the error-free simulations associated with the realization of the lowpass and passband filters of the gyro interface circuitry. Subsequently, two different simulation scenarios, concerning offline and online reconfiguration, demonstrate the ability of our architecture to cope with faults. The ideal FIR filters have been implemented in matlab. The lowpass filter presents a passband-tolerance of 1 db, a stopband attenuation of 35 db at 0.1156 rad/s, while the passband stops at 0.1 rad/s. Table 1 shows the specification of the ideal passband filter. Figures 6 and

7 depict the genetically implemented ones. From the results it is obvious that our architecture is capable to precisely match the desired specification.

Table 1. Passband specification

1 st stopband edge	0.1 rad/s
2 nd stopband edge	0.4 rad/s
Stopband attenuation	20db
1 st passband edge	0.112 rad/s
2 nd passband edge	0.388 rad.s
Passband tolerance	1 db

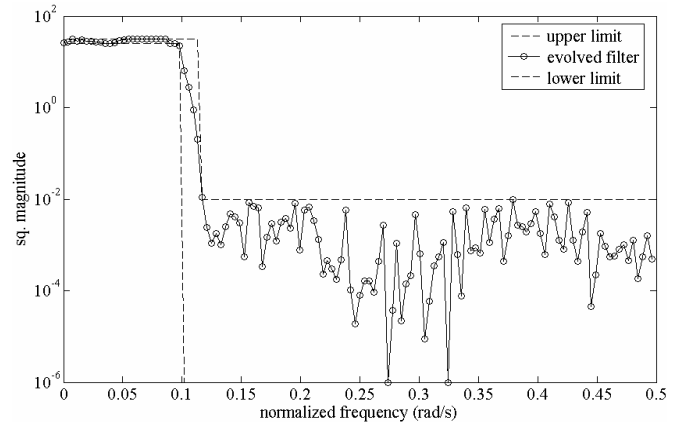


Figure 6. Lowpass filter evolution

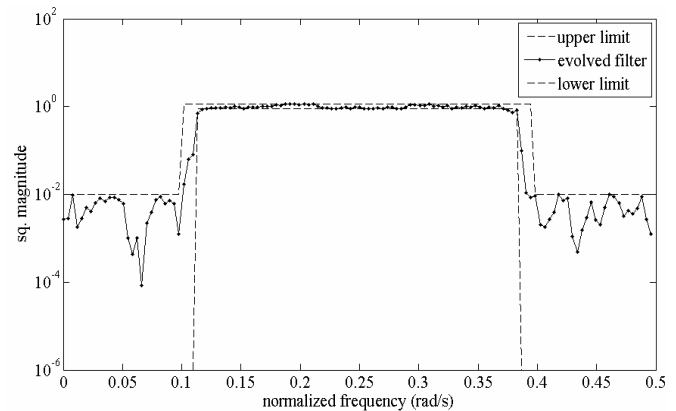


Figure 7. Passband filter evolution

4.1. Offline-reconfiguration

In this simulation scenario, we monitor the performance of the GA for implementing within a faulty environment, the passband filter (figure 8) specified in table 1. Three scenarios of faults equal to 0%, 5% and 10% were injected into the configuration and user memory of the RA. The faults have been introduced from the start of the evolution and are modeled as multiple single-hard-errors (SHEs), which cause permanent changes to the operation of the device.

4.2. Online-reconfiguration

Online reconfiguration presents the ability of our system to recover its functionality in the presence of SHEs. The faults are injected into the system after the filters have been implemented. Figures 9 and 10 demonstrate two different simulations, which illustrate how efficiently the functionality of the passband and lowpass filter is recovered. The two simulations run a limited number of generations (200) because the time required for the online reconfiguration must be shorter than the update rate of the gyro.

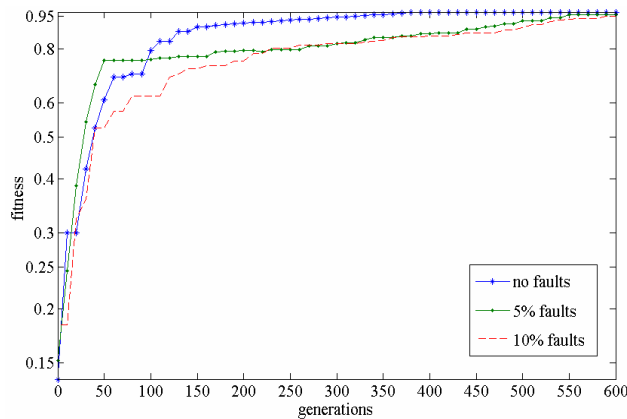


Figure 8. Passband evolution for faults 0, 5 & 10%

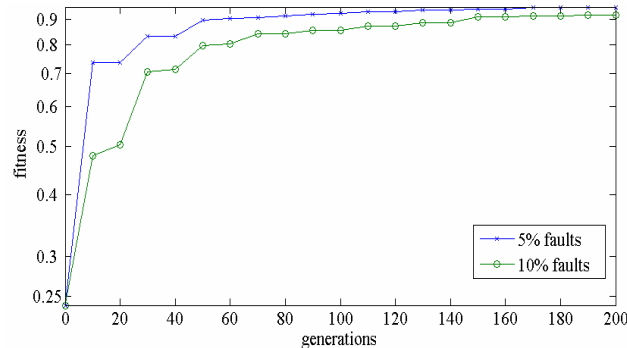


Figure 9. Passband filter recovery for faults 5 & 10%

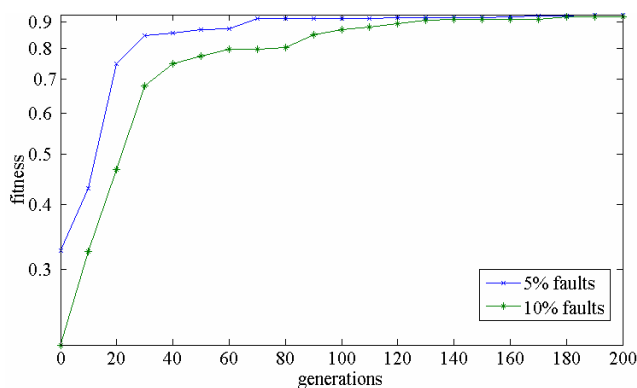


Figure 10. Lowpass filter recovery for faults 5 & 10%

5. Synthesis and power analysis

Our design was synthesized using UMC 0.13 μ m technology cell library. Interconnect parasitics were taken into account in order to obtain a more realistic result. From figure 4, it can be deduced that power savings can be achieved even in active CALBs. This is feasible because the control-bit of the 2 multiplexers inside each CALB can control the enable-bit of the matching registers. Initially both filters consume approximately the same power, which is equal to 0.3767mW/MHz. However, after disabling the redundant component, the lowpass filter consumes 0.2767mW/MHz, while the passband one consumes 0.256mW/MHz. Finally, the achieved power results make our RA very competitive compared with ATMEL 6000 series FPGAs [5].

6. Conclusions

This paper presents a novel architecture that has been designed for the implementation of FIR filters, which require continuous adaptation due to environmental changes. Our system was demonstrated through the representative example of the JPL/Boeing MEMS gyroscope. The obtained results show that the system provides enough adaptability and robustness to cope with occurring of faults up to 10%. Power analyses of the simulated netlists prove that our customized design secures significantly lower power-consumption compared with commercial FPGAs.

7. References

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