

The Design of Optimized Programmable Transmitter and Receiver Architectures for an Integrated Sensor Microsystem

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Abstract

Utilization of wireless miniaturized electronic systems in medical diagnosis has been made possible by emergence of system-on-chip technology. Communication systems targeting miniaturized sensor microsystem networks are characterized by their restricted power and area constraints. When considering the design of telecommunication system for such a network the receiver is the key performance critical block. This paper describes research work carried out on studying the impact of input data characteristics and internal data path complexity on area and power performance of the receiver. We have designed a number of optimized programmable transmitter and receiver architectures specifically for an integrated microsystem and studied their power/area characteristics. We demonstrate that up to 59% and 11% savings in area and power respectively could be achieved by optimizing input data size and internal register width for a particular application while maintaining signal quality and a certain degree of programmability.

Introduction

There has been a general interest in the development of miniaturized and low-power integrated sensor microsystems in many application fields such as medical diagnosis (1), environmental monitoring (2), and biomedical telemetry (3). The emergence of system-on-chip (SoC) technology (4) has produced a potential for significantly shrinking the size of silicon based systems; while enhancing their performance and functionality. The microsensor system described in this paper is in the form of an ingestible electronic capsule (5), which integrates several sensors, amplifiers, analog digital conversion, and includes microsystem scheduling, coding and transmitting circuitry (6) (7). The system is able to monitor some common physiological parameters of gastro-intestinal tract such as temperature, pH, conductivity, and oxygen concentration. One of the main problems of such a system is how to retrieve these information from the sensor system in real-time. The most feasible solution is to integrate a wireless communication circuit into the system. This constitutes an important part of a SoC implementation. Some of the desirable properties of the communication system are capability of communicating with multiple sensor systems for the purpose of centrally monitoring/controlling more than one medium

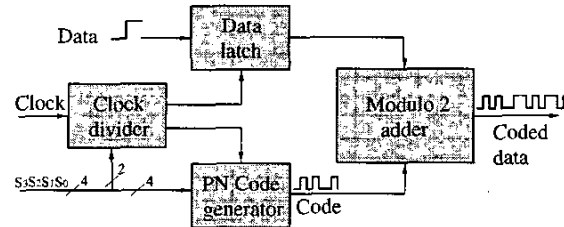


Fig. 1. Block diagram of the programmable DS-SS transmitter.

at the same time and interference rejection for reliable communication in critical applications such as medical diagnosis.

A direct sequence spread spectrum (DS-SS) based communication system for an integrated sensor microsystem, which fulfills these requirements, has been recently described (8). When considering the design of telecommunication system for such a network the receiver is the key performance critical block as the receiver is much more complicated than the transmitter. In this paper we present design of optimized programmable transmitter and receiver architectures specifically for an integrated microsystem and studied their power/area characteristics for various input data width and system dynamic ranges. We also present some qualitative test results from the actual chip, which was fabricated.

This paper is organized as follows. In Section 2 we discuss DS-SS transmitter and receiver implementation. In Section 3 we then describe extensive power evaluations of the receiver design for various input data width and system dynamic ranges (internal register width). Finally we summarize our major findings and outline our future work.

TABLE I
CODE SELECTION FOR TRANSMITTER
AND RECEIVER

$S_3S_2S_1S_0$	Feed-back	Code length	$S_3S_2S_1S_0$	Feed-back	Code length
0000	No Coding	-	1000	Reserved	-
0001	[5,2]	32	1001	[7,1]	128
0010	[5,4,3,2]	32	1010	[7,3]	128
0011	[5,4,2,1]	32	1011	[7,3,2,1]	128
0100	Reserved	-	1100	Reserved	-
0101	[6,1]	64	1101	[8,4,3,2]	256
0110	[6,5,2,1]	64	1110	[8,6,5,3]	256
0111	[6,5,3,2]	64	1111	[8,6,5,2]	256

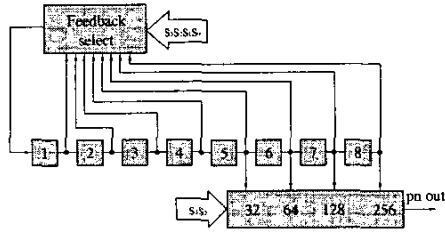


Fig. 2. Structure of the programmable LFSR based PN generator.

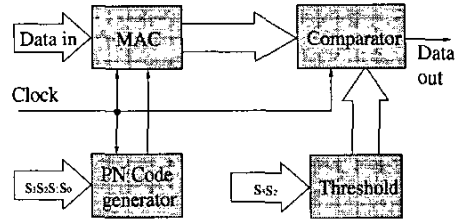


Fig. 3. Block diagram of the DS-SS receiver.

Design and Implementation

A Transmitter Design

The heart of the DS-SS transmitter is the PN generator, which is based on Linear Feedback Shift Registers (LFSR) (9) (10). A PN sequence is a binary sequence that exhibits randomness properties but has a finite length and is therefore deterministic. They are used to implement synchronization and uniquely code individual user signals across the transmission interface. The data is spread by multiplying with the PN code. Block diagram of the programmable transmitter is given in Fig. 1. It comprises a memory block for storage of data, a programmable PN code generator block consisting eight stages LFSR and a multiplexer, a clock divider providing appropriate clock for the memory block and the PN generator, and a block of logic gates to perform the data coding and spreading.

The PN code length is programmable to provide appropriate spreading amount of data for a particular application. Available code lengths are 32, 64, 128, and 256. Three different PN codes for each code lengths are available depending on the code select inputs. Available PN code options are given in Table 1. The required feed-back combination for a particular PN code is selected by a multiplexer. The structure of the programmable LFSR based PN generator is illustrated in Fig. 2. The transmitter described here was fabricated as part of an integrated sensor microsystem [6].

B. Receiver Design

A DS-SS receiver, which is based on a correlator, exploits correlation properties of the PN codes (10). The correlators attempt to match the incoming received signal with each of the candidate prototype waveforms known *a priori* to the receiver. The discrete form of the correlation of two discrete signals is given as

$$r_{xy}(k) = \sum_{n=0}^{N-1} x(n)y(k+n) \quad (1)$$

Equation (1) is the fundamental equation implemented in software and hardware. The implementation of a correlator is based on a multiplier-accumulator circuit (MAC). If the PN code and the incoming signal are identical, the correlator output will yield a positive peak output at zero phase shifts. If the input signal is 180 degree out of phase the correlator output will yield a negative peak output. Then a threshold function recovers the original data. At other phases, the output of correlator will ideally be zero. However this is the case when the PN code length is infinite, which is

unrealizable. In practice a finite length of PN code is used. Therefore there is a certain degree of correlation between incoming signal and the PN code at phases other than zero. Since the incoming signal is no longer a simple digital signal due to distortions caused by many noise sources such as channel distortion, multiple access distortion, and additive white Gaussian noise, the incoming signal must be demodulated and digitized. Therefore, the DS-SS receiver must employ a proper computational circuitry such as multiplier and accumulator. The block diagram of the receiver is illustrated in Fig. 3. The same PN code generator as in the transmitter is used. In fact the PN code has only two values; 0 or 1. This corresponds to +1 and -1 in bipolar format. Implication of this is that multiplication of the DS-SS coded input data and PN code is no more than that a sign modification. As a result the receiver circuit reduces to a simple adder or subtractor depending on the PN code value. Addition and subtraction use the same circuit when two's complement arithmetic is used, leading to further simplification of the receiver design. Figs. 4(a) and 4(b) illustrate an example of normalized transmitted and received test signals respectively. The signal was originally recorded from an intravascular pressure sensor. Fig. 4(c) illustrates the difference between the original and the reconstructed pressure waveform. This difference is mainly caused by the quantization. The data were digitized by an 8 bit A/D converter modeled in Matlab and converted into a bit stream, then coded and transmitted. Simulations were performed in Verilog environment at netlist level.

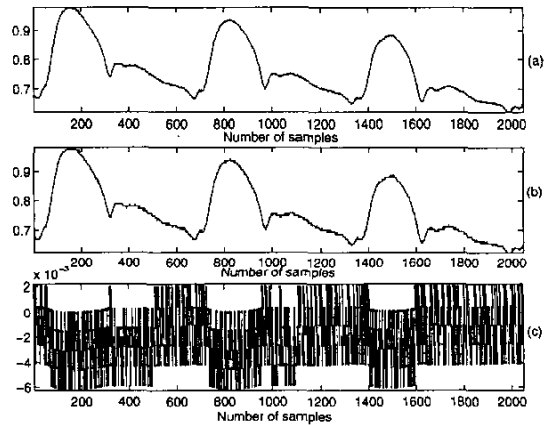


Fig. 4. (a) Original test data from an intravascular pressure sensor, (b) reconstructed test data at the receiver, and (c) the difference between original signal and reconstructed signal.

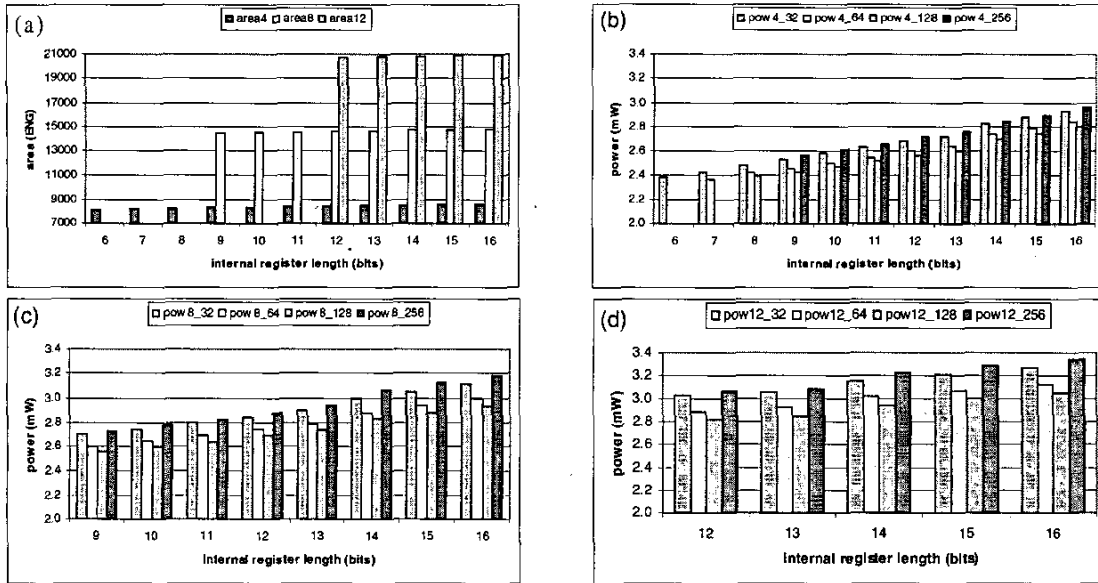


Fig. 5. Area and power estimations of the receiver as a function of input data and internal register width.
 ENG: equivalent NAND gate
 area4(8)(12): receiver core area with the input data width of 4(8)(12) bits
 pow4(8)(12)_32(64)(128)(256): power estimation with the PN code length of 32(64)(128)(256) and the input data width of 4(8)(12) bits

Design Considerations and Optimization

A. Power Evaluation

Comparing to the receiver, transmitter implementation is not complicated. So, the power consumption of the transmitter is extremely low compared to the receiver (8). Impact of the transmitter's power consumption on overall sensor microsystem is insignificant. Assuming the clock frequency is fixed, the transmitter power and area is only a function of the PN code length. On the other hand the receiver power and area may greatly be influenced by the choice of input data width and the internal register width of accumulator as well as the PN code length. Power consumption and area of the receiver are much more critical if a duplex communication capability is needed in an integrated sensor microsystem. Therefore in order to investigate the impact of the input data size, we assumed that the data was digitized by 4, 8, and 12 bit ADC in each case. In the first case (4 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 6 to 16 bits, each for 4 different PN code lengths (32, 64, 128, and 256). In the second case (8 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 9 to 16 bits, each for 4 different PN code lengths. In the last case (12 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 12 to 16 bits, again each for 4 different PN code lengths.

B. Simulations and Results

The transmitter and the receiver for each input data widths and internal register widths were synthesized

using Synopsys Design Compiler and Alcatel 0.35u technology. Netlist simulations were performed using Cadence's Verilog-XL simulator for each case. Simulation results are presented in Fig. 5. Assuming a 10 MHz operating frequency and 3 Volts power supply, first a test data given as '10101010' was coded by the transmitter using each PN length. Then the transmitted signals were digitized as described above in Matlab. The digitized signals were then used by the receiver considering three input data widths and all the possible internal register widths up to 16 bits as mentioned above. The switching activity information obtained from the netlist simulations was fed into the Synopsys Design Power and total power consumptions were estimated. Area and comparative power estimations of the receiver for all the combinations of input data width and internal register widths are illustrated in Fig. 5. Although the receiver core area linearly increases by increasing internal register length, it is mainly a function of input data width (Fig. 5(a)). That is to say that the memory block takes most of the space in the correlator. This has an important implication on the applications with area constraints such as described in this paper. Therefore in area constrained SoC applications, utilization of unnecessarily higher resolution ADCs for the correlator receiver should be avoided. Fig. 5(b) shows power figures when the input data width is 4 bits. In this case, the minimum internal register length, which will not cause saturation in accumulator, is 6 bits with a PN code length of 32, 7 bits with a PN code length of 64, 8 bits with a PN code length of 128, and 9 bits with a PN code length of 256. Although power consumption increases linearly with increasing register lengths, it is insignificant. Figs. 5(c) and 5(d) show the estimation of the powers when the input data width is 8 and 12 bits respectively. In those cases, internal register sizes less

than 9(12) bits for 8(12) bit input data will cause saturation in the accumulator. Again power consumptions increase linearly with increasing register lengths and are insignificant. For a safe data reception, therefore the internal register size in the programmable receiver described here should be at least 9 bits when the input data width is 4 and 8 bits, and 12 bits when the input data width is 12 bits.

From the experimental results presented here it can be concluded that for very specialized implementations requiring the lowest possible power consumption, ideally the design with minimum register size should be considered. However if a certain degree of programmability and input data flexibility is required, then the size of the internal register length should be at least 12. This will also assure in practice that the accumulator will not saturate as a result of unexpected input signal fluctuations.

Summary

We have designed and implemented a DS-SS based transmitter and receiver incorporating a certain degree of programmability as part of a SoC implementation. We also have performed extensive power and area evaluations in order to determine the optimized transmitter and receiver designs for an integrated sensor microsystem, which measures approximately 30x12 mm. Based on the experimental results presented here, in our application considerable amount of area and power (up to 59% and 11% respectively) can be saved by optimizing the input data width and internal register size for a particular application. Currently, the first generation of the integrated sensor microsystem consisting of the DS-SS based transmitter described above has been assembled and is undergoing in-vivo tests. The SoC of the second generation of the system has been tested for functionality. Fig. 6 illustrates normalized autocorrelation results of the actual on-chip transmitter outputs recorded by a digital scope for PN length of 256, 128, 64, and 32. The main challenge is to incorporate a highly complex programmable receiver on the integrated microsensor system. It is expected that the utilization of the observations presented in this paper in the next generation of the integrated sensor microsystem will enable us to increase functionality while reducing power consumption and area and perhaps to include a DS-SS receiver in the SoC in our future work. For example, a new design with more advanced functions allowing software controllable transmission with same power and area has already been submitted for fabrication.

Acknowledgment

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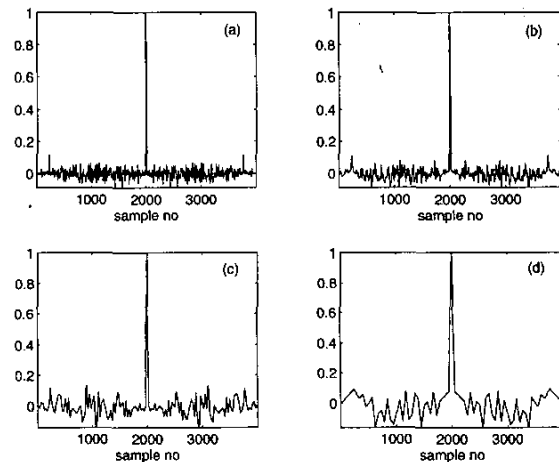


Fig. 6. Normalized autocorrelation results of the actual on-chip transmitter outputs recorded by a digital scope for the PN length of (a) 256, (b) 128, (c) 64, and (d) 32.

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