

Power/Area Analysis and Optimization of a DS-SS receiver for an Integrated Sensor Microsystem

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Abstract

Communication systems targeting miniaturized sensor microsystem networks are characterized by their restricted power and area constraints. When considering the design of telecommunication system for such a network, the receiver is the key performance critical block. This paper describes research work carried out on studying the impact of input data characteristics and resolution and internal data path complexity on area and power performance of the receiver. We have constructed a number of transmitter/receiver architectures and analyzed their power/area. We demonstrate that up to 59% and 11% savings in area and power respectively could be achieved by optimizing input data size and internal register width for a particular application while maintaining signal quality.

1. Introduction

There has been a general interest in the development of miniaturized and low-power integrated sensor microsystems [8][23] in many application fields such as medical diagnosis [1], environmental monitoring [10], and biomedical telemetry [13][14]. The emergence of system-on-chip (SoC) technology [11] has produced a potential for significantly shrinking the size of silicon based systems, while enhancing their performance and functionality [19]. The microsensor system described in this paper is in the form of an ingestible electronic capsule [22][24], which integrates several sensors, amplifiers, analog digital conversion, and includes microsystem scheduling, coding and transmitting circuitry. The system is able to monitor some common physiological parameters of gastro-intestinal tract such as temperature, pH, conductivity, and oxygen concentration.

One of the main problems of such a system is how to retrieve these information from the sensor system in real-time. The most feasible solution is to integrate a wireless communication circuit into the system, which constitutes an important part of a SoC implementation [5][25]. Some of the desirable properties of the communication system are capability of communicating with multiple sensor systems for the purpose of centrally monitoring/controlling more than one medium at the same time and interference rejection for reliable communication in critical applications such as medical diagnosis. Direct sequence spread spectrum (DS-SS) communication system can fulfill these requirements [3][4]. A DS-SS based communication system, which was designed specifically for an ingestible capsule intended for medical diagnosis, has been recently reported [2]. In this paper we present extensive power evaluations of the design for various input data width and system dynamic ranges.

This paper is organized as follows. In Section 2 we discuss DS-SS transmitter and receiver implementation. In Section 3 we then describe extensive power evaluations of the receiver design for various input data width and system dynamic ranges (internal register width). Finally we summarize our major findings and outline our future work.

1.1 Multiple Access Systems

One of the applications of spread spectrum signals is to multiple access systems. In a multiple access system, a number of users share a common channel to transmit information. Within a communication system we have a fixed amount of resources, a fixed amount of spectrum, a fixed amount of equipment, and a fixed number of channels. We also have multiple subscriber units which are trying to access the system at the same time. The system has to manage resources appropriately in

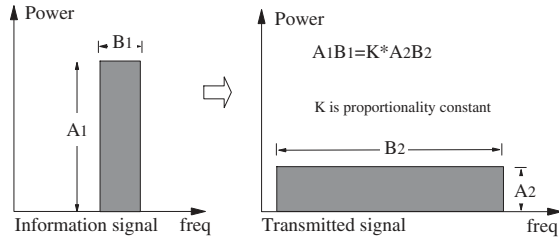


Figure 1. Frequency spreading in DS-SS.

order to cover and support all the users that want to access the system. There are three common technologies used to create an air interface; frequency-division multiple access (FDMA), time-division multiple access (TDMA), code-division multiple access (CDMA) [21]. In FDMA, the available channel bandwidth is subdivided into a number of frequency nonoverlapping channels. These subchannels are assigned to each user upon request by the users. FDMA allocates a single channel to one user at a time. Although technically simple to implement, FDMA is wasteful of bandwidth. TDMA relies upon the fact that the signal has been digitized; that is, divided into a number of packets. It allocates a single frequency channel for a short time and then moves to another channel. The digital samples from a single transmitter occupy different time slots in several bands at the same time. The main drawback is that with narrower bandwidth there is greater distortion. In an environment where the transmission from the various users is bursty and low duty cycle, FDMA and TDMA tend to be inefficient because a certain percentage of the available frequency slots or time slots assigned to user do not carry information [17]. This inefficiency in a multiple access system limits the number of simultaneous users of the channel. An alternative to FDMA and TDMA is to allow more than one user to share a channel by use of DS-SS signals [20] [15].

1.2 Direct Sequence Spread Spectrum

In the DS-SS system, each user is assigned a unique code sequence [6] that allows the user to spread the information signal across the assigned frequency band. Signals from the various users are separated at the receiver by cross-correlation of the received signal with each of the possible user code sequences. Possible narrow band interference is also suppressed in this process. By designing these code sequences to have relatively small cross-correlation, the cross-talk inherent in the demodulation of the signals received from multiple transmitters is minimized. This multiple access

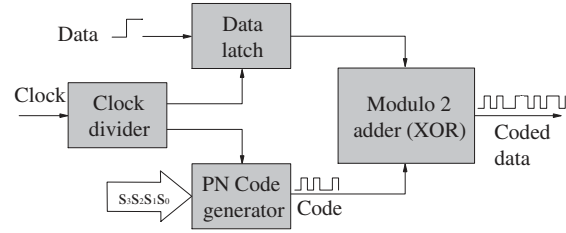


Figure 2. Block diagram of the DS-SS transmitter.

method is CDMA [18] [16] [12], which is a form of a DS-SS system. It is the spectral spreading of the transmitted signal that gives CDMA its multiple access capability. In order to classify a system as spread spectrum (SS) modulated system, the transmission bandwidth must be much larger than the information bandwidth and the resulting RF bandwidth must be determined by a function other than the information being sent. The SS modulation transforms an information-bearing signal into a transmission signal with a much larger bandwidth. This transformation is achieved by encoding the information signal with a code signal that is independent of the data and has much larger spectral width than the data signal. This spreads the original signal power over a much broader bandwidth, resulting in a lower power density, as depicted in Figure 1. The ratio of transmitted bandwidth to information bandwidth is called the processing gain G_p of the SS system:

$$G_p = \frac{B_t}{B_i} \quad (1)$$

where B_t is the transmission bandwidth and B_i is the bandwidth of the information bearing signal.

In DS-SS transmitter, the data is spread by multiplying with a Pseudo-random Noise (PN) code. A PN code is a binary sequence that exhibits randomness properties but has a finite length and is therefore deterministic. They are used to implement synchronization and uniquely code individual user signals across the transmission interface. PN generators are based on Linear Feedback Shift Registers (LFSR) [7]. The sequence that an n stage LFSR produces is called maximal LFSR sequence or M-sequence. The length of such sequence is defined as $L = 2^n - 1$ and the number of independent M-sequences (S), for a given length of shift register is defined as $S = (L - 1)/n$. The multiplication process is a simple modulo-2 addition. This multiplication also acts as a phase modulator. In practice, the data is transmitted by using bipolar format

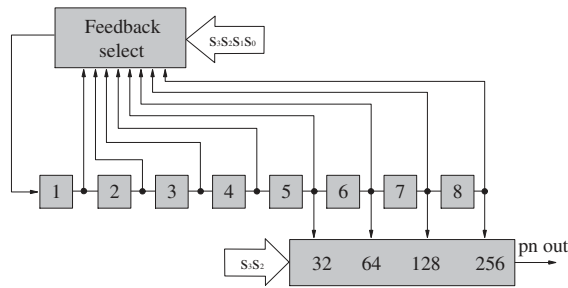


Figure 3. Structure of the programmable LFSR based PN generator.

for convenience. Binary '1' is represented by '-1', and binary '0' by '+1'. This convention will eliminate the *dc* component of the signal.

DS-SS receiver, which is based on a correlator, exploits correlation properties of the PN codes [7]. Suppose $x(t)$ and $y(t)$ are two real functions. Cross-correlation of these two functions is given as

$$r_{xy}(\tau) = \int_{-\infty}^{+\infty} x(t)y(t + \tau)dt \quad (2)$$

If $y(t) = x(t)$, then (2) becomes auto-correlation of $x(t)$. The correlators attempt to match the incoming received signal with each of the candidate prototype waveforms known *a priori* to the receiver. In fact, it is a measure of similarities of two signals. Since we deal with the discrete signals in practice, the discrete form of the correlation of two discrete signals is given as

$$r_{xy}(k) = \sum_{n=0}^{N-1} x(n)y(k + n)dt \quad (3)$$

Equation (3) is the fundamental equation implemented in software and hardware. The hardware implication of (3) is that the implementation of a correlator is based on a multiplier-accumulator circuit (MAC). At the receiver, the same PN code used in transmitter is correlated with incoming signal. Assuming an ideal transmission, if the PN code and the incoming signal are identical, the correlator output will yield a positive peak output at zero phase shifts. If the input signal is 180 degree out of phase the correlator output will yield a negative peak output. Then a threshold function recovers the original data. At other phases, the output of the correlator will ideally be zero. However this is the case when the PN code length is infinite, which is unrealizable. In practice a finite length of PN code is used. Therefore there is a certain degree of correlation

Table 1. Code selection for transmitter and receiver

$s_3s_2s_1s_0$	Feed-back	PN Code length
0 0 0 0	No Coding	-
0 0 0 1	[5,2]	32
0 0 1 0	[5,4,3,2]	32
0 0 1 1	[5,4,2,1]	32
0 1 0 0	Reserved	-
0 1 0 1	[6,1]	64
0 1 1 0	[6,5,2,1]	64
0 1 1 1	[6,5,3,2]	64
1 0 0 0	Reserved	-
1 0 0 1	[7,1]	128
1 0 1 0	[7,3]	128
1 0 1 1	[7,3,2,1]	128
1 1 0 0	Reserved	-
1 1 0 1	[8,4,3,2]	256
1 1 1 0	[8,6,5,3]	256
1 1 1 1	[8,6,5,2]	256

between incoming signal and the PN code at phases other than zero.

2. Design and implementation

2.1. Transmitter design

The heart of the DS-SS transmitter is the PN generator, which is based on LFSR [7][6]. The data is spread by multiplying with the PN code. In practice, the multiplication is a simple modulo-2 addition, which also acts as a phase modulator. Block diagram of the transmitter is given in Figure 2. It comprises of a memory block for storage of data, a programmable PN code generator block consisting eight stages LFSR and a multiplexer, a clock divider providing appropriate clock for the memory block and the PN generator, and a block of logic gates to perform the data coding and spreading. The PN code length is programmable (32, 64, 128, or 256) to provide appropriate spreading amount of data for a particular application. One of the 12 different codes (3 for each length) is available depending on the code select inputs, as given in Table 1. The structure of the programmable LFSR based PN generator is illustrated in Figure 3. The data is transmitted by using bipolar format, which eliminates the *dc* component of the signal and has also a significant implication in the receiver design.

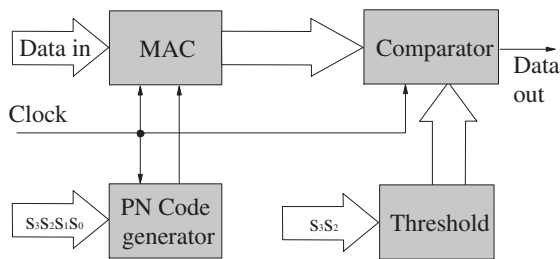


Figure 4. Block diagram of the DS-SS receiver.

2.2. Receiver design

A DS-SS receiver, which is based on a correlator, exploits correlation properties of the PN codes [7]. The correlators attempt to match the incoming received signal with each of the candidate prototype waveforms known a priori to the receiver. The implementation of a correlator is based on a MAC. Assuming perfect synchronization and no channel distortion, DS-SS receiver is no more complicated than the transmitter except for few extras namely accumulator and comparator. However, in reality the incoming signal is no longer a simple digital signal due to distortions caused by many noise sources such as channel distortion, multiple access distortion, and additive white Gaussian noise. Moreover, DS-SS coded signal is modulated with a carrier and transmitted as an analog signal. At the receiver side, the incoming signal must be demodulated and digitized. Therefore, the DS-SS receiver must employ a proper computational circuitry such as multiplier and accumulator. The block diagram of the receiver is illustrated in Figure 4. The same PN code generator as in the transmitter is used. In fact the PN code has only two values; 0 or 1. This corresponds to +1 and -1 in bipolar format. Implication of this is that multiplication of the DS-SS coded input data and PN code is no more than that a sign modification. That is to say the multiplier is redundant. As a result the receiver circuit reduces to a simple adder or subtractor depending on the PN code value. Addition and subtraction use the same circuit when two's complement arithmetic is used. This further simplifies the receiver design.

Figure 5 illustrates the operation of the transmitter and the receiver by using 1000 test data recorded from a pH sensor, which was a component of an integrated sensor microsystem [24]. The data were digitized by an 8 bit A/D converter modeled in Matlab and converted into a bit stream, then coded and transmitted. The original test data is illustrated in Figure 5(a). The pH

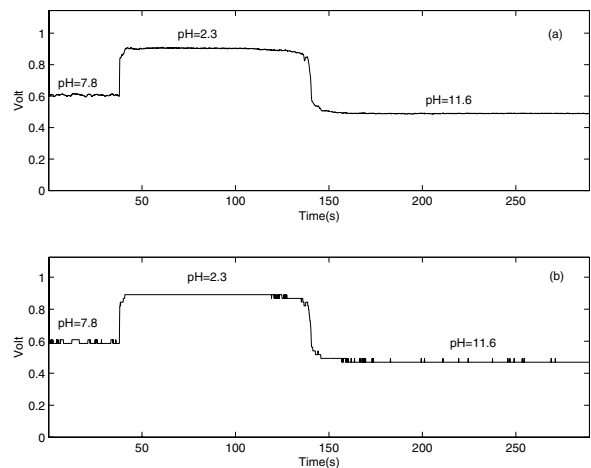


Figure 5. (a) Original test data from the pH sensor, (b) reconstructed test data at the receiver.

scale, which measures hydrogen-ion concentration, is a notation that extends from 0 to 14 with 7 as its middle point [9]. The reconstructed data at the receiver is shown in Figure 5(b).

3. Power evaluation

3.1. Implementation considerations

Unlike the receiver, the transmitter implementation is straightforward and not complicated. So the power consumption of the transmitter is quite low compared to the receiver [6]. Assuming the clock frequency is fixed, the transmitter power and area is a function of the PN code length. However the receiver power and area may greatly be influenced by the choice of input data width and the internal register width of accumulator as well as the PN code length. Therefore we assumed that the data was digitized by 4, 8, and 12 bit ADC in each case. In the first case (4 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 6 to 16 bits, each for 4 different PN code lengths (32, 64, 128, and 256). In the second case (8 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 9 to 16 bits, each for 4 different PN code lengths. In the last case (12 bits), power consumptions and areas of the receiver were evaluated for internal register widths from 12 to 16 bits, again each for 4 different PN code lengths.

3.2. Simulations and results

The transmitter and the receiver for each input data width and internal register width were synthesized using *Synopsis Design Compiler* and *Alcatel 0.35 μ* technology. Netlist simulations were performed using Cadence's Verilog-XL simulator for each case. Assuming a 10 MHz operating frequency and 3 Volts power supply, first a test data given as 10101010 was coded by the transmitter using each PN length. Then the transmitted (coded) signals were digitized as described above in *Matlab*. The digitized signals were then used by the receiver considering three input data widths and all the possible internal register widths up to 16 bits as mentioned above. The switching activity information obtained from the netlist simulations was fed into the *Synopsis DesignPower* and total power consumptions were estimated. Area and comparative power estimations of the receiver for all the combinations of input data width and internal register widths are illustrated in Figure 6. Although the receiver core area linearly increases by increasing internal register length, it is mainly a function of input data width (Figure 6(a)). That is to say that the memory block takes most of the space in the correlator. This has an important implication on the applications with area constraints such as described in this paper. Therefore in area constrained SoC applications, utilization of unnecessarily higher resolution ADCs for the correlator receiver should be avoided. Figure 6(b) shows power figures when the input data width is 4 bits. In this case, the minimum internal register length, which will not cause saturation in accumulator, is 6 bits with a PN code length of 32, 7 bits with a PN code length of 64, 8 bits with a PN code length of 128, and 9 bits with a PN code length of 256. Although power consumption increases linearly with increasing register lengths, it is insignificant. Figures 6(c) and 6(d) show the estimation of the powers when the input data width is 8 and 12 bits respectively. In those cases, internal register sizes less than 9(12) bits for 8(12) bits input data will cause saturation in the accumulator. Again power consumptions increase linearly with increasing register lengths and insignificant. For a safe data reception, therefore the internal register size in the programmable receiver described here should be at least 9 bits when the input data width is 4 bits and 8 bits, and 12 bits when the input data width is 12 bits.

From the experimental results presented here it can be concluded that for very specialized implementations requiring the lowest possible power consumption, ideally the design with minimum register size should be considered. However if a certain degree of programma-

bility and input data flexibility is required, then the size of the internal register length should be at least 12. This will also assure in practice that the accumulator will not saturate as a result of unexpected input signal fluctuations.

4. Summary

We have designed and implemented a DS-SS based transmitter and receiver incorporating a certain degree of programmability as part of a SoC implementation. We also have performed extensive power and area evaluations in order to determine the optimized transmitter and receiver design for an integrated sensor microsystem, which measures approximately 30 \times 12 mm. Based on the experimental results presented here, in our application considerable amount of area and power (up to 59% and 11% respectively) can be saved by optimizing the input data width and internal register size. Currently, the first generation of the integrated sensor microsystem has been assembled and is undergoing in-vivo tests. The SoC ASIC of the second generation of the system is being tested for functionality. It is expected that the utilization of the observations presented in this paper in the next generation of the integrated sensor microsystem will help us to increase functionality while reducing power consumption and area of the integrated sensor microsystem

5. Acknowledgment

This work was supported by the Scottish Higher Education Founding Council (RDG 130).

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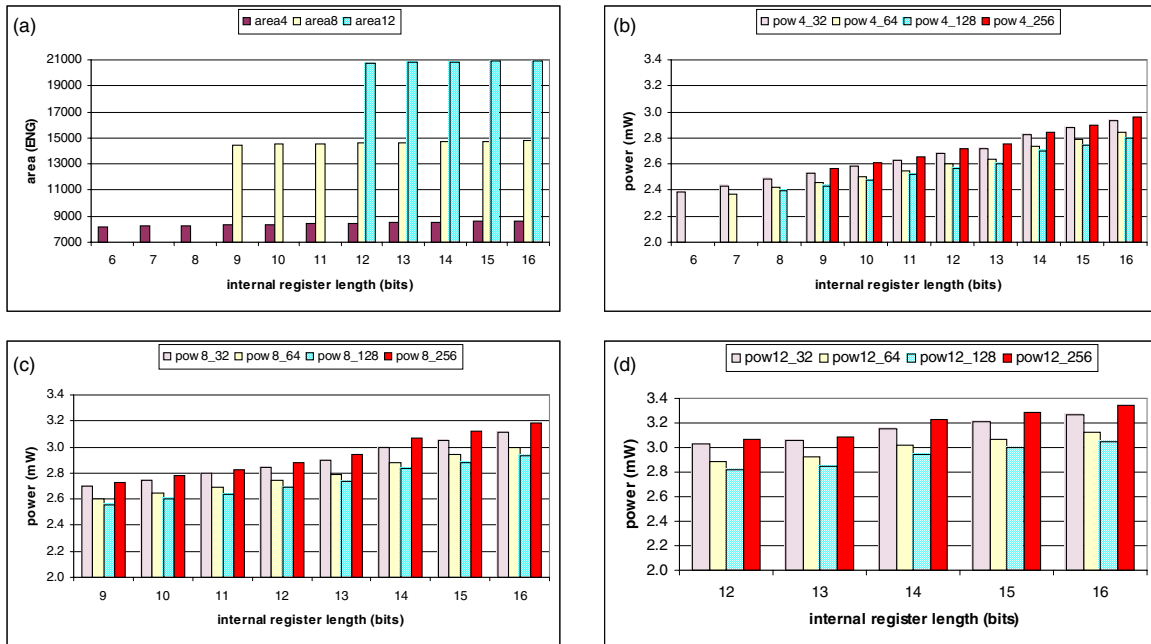


Figure 6. Area and power estimations of the receiver as a function of input data and internal register width.(ENG: equivalent NAND gate; $area4(8)(12)$: receiver core area with the input data width of 4(8)(12) bits; $pow4(8)(12)_{32(64)(128)(256)}$: power estimation with the PN code length of 32(64)(128)(256) and the input data width of 4(8)(12) bits)

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