

The DQHA was also evaluated in comparison with a microstrip patch antenna. This measurement was undertaken to evaluate the effect of the balun isolation for the DQHA. In this part of the research, each antenna was measured attached to a Nokia 5110 mobile telephone in the presence of a phantom human hand. The patch antenna was not connected to the mobile telephone ground, but cabled through the battery pack, yielding an improved measurement.

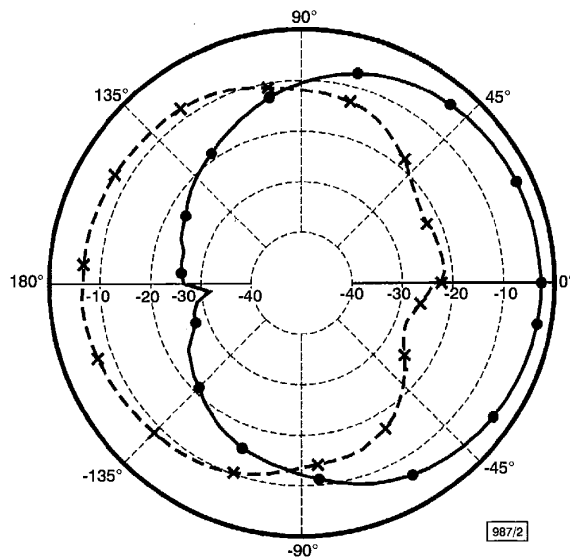


Fig. 2 Right and left hand circular polarisation patterns at 1575.42 MHz

—●— right hand
-x- left hand

Left and right hand circular polarisation patterns (without a ground plane) at 1575.42 MHz are shown in Fig. 2. At this frequency, the two circular polarisation patterns show 19.6 dB discrimination between left and right hand polarisations in boresight. The DQHA has a gain of -2 dBi with a radiation efficiency of 25%. The axial ratio shows a minimum of 0.99 dB at 1575.42 MHz.

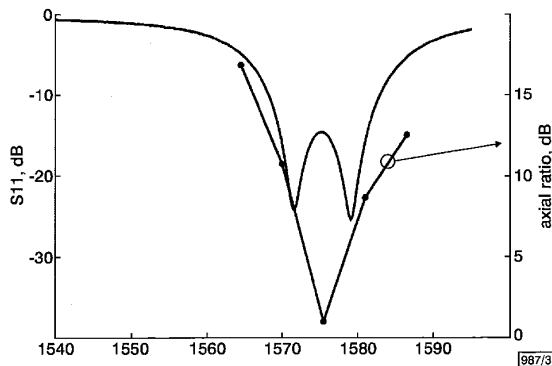


Fig. 3 Axial ratio and return loss of DQHA

Fig. 3 shows values for the axial ratio of the DQHA at five frequencies centred around the GPS L1 frequency. Also plotted is the S_{11} for the DQHA. These data demonstrate the principle of two coupled resonances slightly off the desired frequency to give the required phase differential between the two helix paths. The optimum axial ratio (0.99 dB) is at the GPS L1 frequency, which corresponds to the saddle point (-14.6 dB) of the S_{11} measurement.

Fig. 4 shows a comparison of the two antennas, which are considered suitable for mobile handset GPS applications. The antennas are a dielectrically-loaded patch antenna (of comparable size) and the reported DQHA antenna. The patterns are for the antennas attached to the handset in close proximity with the phantom hand. The patch antenna gain dropped from 0 dBi (free space) for a 1 inch by 1 inch groundplane to -3.5 dBi when placed on a mobile telephone loaded with a phantom hand. The DQHA showed a reduction of gain from -2 to -3 dBi in similar circum-

stances. Equally as important, the DQHA demonstrated, and maintained, a far superior front-to-back ratio over the patch antenna.

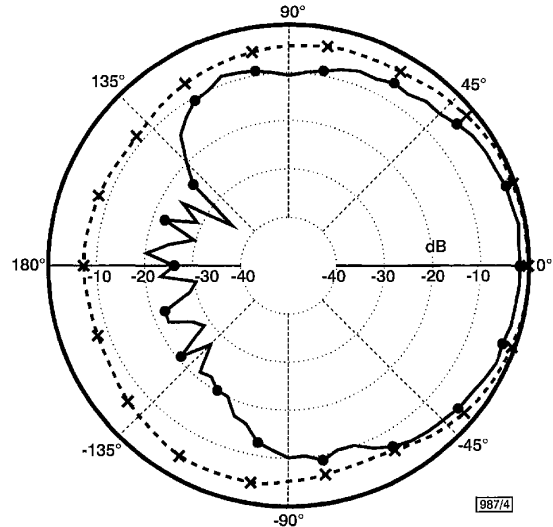


Fig. 4 Comparison of patch and DQHA mounted on mobile telephone in close proximity to phantom hand

—●— DQHA
-x- patch antenna

The results reported here show that the DQHA is not affected significantly by the handset and the phantom human hand. Furthermore, the fact that the electromagnetic fields are contained in the dielectric core means that this type of antenna can work in close proximity to other antennas on a handset without significant interaction. The DQHA can conveniently be mounted on a mobile telephone.

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Coefficient memory addressing scheme for high performance FFT processors

M. Hasan and T. Arslan

A novel scheme for coefficient address generation in a fast Fourier transform (FFT) processor is presented. The proposed addressing scheme involves manipulation of the address lines taking into consideration coefficient addresses required at various FFT stages. It is demonstrated that the scheme can be implemented more efficiently with much reduced hardware than approaches published to date, leading to faster, more power and area efficient realisation of FFT processors.

Introduction: High performance fast Fourier transform (FFT) processors are widely used in different areas of application such as communications, radars, imaging etc. Enhancing the performance of the FFT is a major concern for researchers. Previously, research has concentrated on speed enhancement; however, with the advent of portable computation, area and especially power consumption have become of particular interest [1].

Memory addressing is a key research concern for enhancing the performance of FFT processors. To date, the most popular and computationally efficient method of coefficient address generation was proposed by Cohen [2]. According to this method, address generation occurs through the application of variable shifts to address lines through a cascade of Barrel shifters. The work in [3] modified the data generation scheme proposed by Cohen while retaining the coefficient address generation method.

In this Letter we present a novel scheme for coefficient address generation in an FFT processor. The proposed addressing scheme involves manipulation of the address lines taking into consideration coefficient addresses required at various FFT stages. We demonstrate that the scheme can be implemented more efficiently with much reduced hardware than the approaches published to date leading to faster, more power and area efficient realisation of FFT processors.

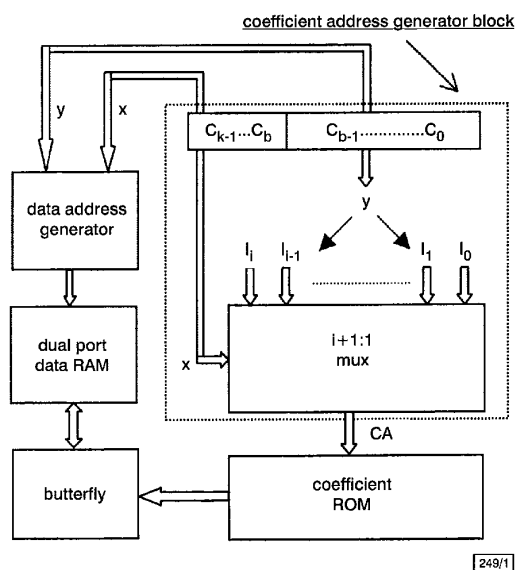


Fig. 1 Hardware block diagram of N -point FFT

Detailed design: The N -point discrete Fourier transform (DFT) is defined by

$$X_k = \sum_{m=0}^{N-1} x_m \cdot W_N^{mk}$$

where $W_N = \exp(-j2\pi/N)$ and $k = 0, 1, \dots, N-1$. The radix-2 FFT [4] is an efficient way to compute an N -point DFT. The basic operations in FFT are multiplication of the complex data inputs by the FFT coefficients ($\exp(-j2\pi k/N)$) at each stage in the signal flowgraph, followed by their summation or subtraction and associated data and coefficient address generation. The coefficient and data address generation logic are required to be fast, area and power efficient in order to realise fast, miniaturised and low power FFT processors which could be integrated into complex very large scale integration (VLSI) systems. In this Letter, the coefficient address generation in an FFT is accomplished by partitioning a k -bit counter into two sections as shown in Fig. 1. The more significant counter section comprises (C_{k-1}, \dots, C_b) bits whereas the lower section has (C_{b-1}, \dots, C_0) bits. Let the more and less significant counter section bits be represented by a $(k-b)$ -bit array \mathbf{x} and a b -bit array \mathbf{y} , respectively. The coefficient address (CA) is then expressed as follows:

$$CA = F(\mathbf{x}, \mathbf{y}) \quad (1)$$

Let us also assume that i = decimal equivalent of \mathbf{x} , which is always greater than or equal to ' b ' depending upon the FFT size, then eqn. 1 can be written as follows:

$$CA = \mathbf{I}_i$$

where \mathbf{I}_i is a b -bit array, which is expressed in terms of an array \mathbf{y} according to the following set of equations:

$$\begin{aligned} \mathbf{I}_0 &= (0 \dots 0) \\ \mathbf{I}_1 &= (\mathbf{y}[b-1]0 \dots 0) \\ \mathbf{I}_2 &= (\mathbf{y}[b-1]\mathbf{y}[b-2]0 \dots 0) \\ &\vdots \\ \mathbf{I}_{b-1} &= (\mathbf{y}[b-1]\mathbf{y}[b-2]\mathbf{y}[b-3] \dots \mathbf{y}[1]0) \\ \mathbf{I}_b &= \mathbf{y} \\ \mathbf{I}_{b+1} &= (X \dots X) \\ &\vdots \\ \mathbf{I}_i &= (X \dots X) \end{aligned} \left. \vphantom{\begin{aligned} \mathbf{I}_0 \\ \mathbf{I}_1 \\ \mathbf{I}_2 \\ \vdots \\ \mathbf{I}_{b-1} \\ \mathbf{I}_b \\ \mathbf{I}_{b+1} \\ \vdots \\ \mathbf{I}_i \end{aligned}} \right\} \text{Not required}$$

where N = size of the FFT, $b = \log_2(N/2)$, X = don't care bit and $k = b + \{\log_2(\log_2(N))$ (rounded up to the nearest integer)}. This set of operations could be realised in hardware by using a single multiplexer-based coefficient address generation logic as shown in Fig. 1. The input channels of the multiplexer are set according to \mathbf{I}_i and selected by \mathbf{x} .

To illustrate this scheme, consider a signal flowgraph of a radix-2 16-point FFT algorithm [3]. In the first stage of the flowgraph, only the first coefficient with an address value 0 (W^0), is required for all eight butterflies. In the second stage, W^0 and W^4 coefficients are required. In the third stage, W^0 , W^2 , W^4 and W^6 coefficients are needed, whereas in the last stage all the coefficients from W^0 to W^7 are required for the butterfly operations. In this example, the coefficient memory has eight locations for storing coefficients (W^0 to W^7) and hence the lower counter section should comprise only three bits, C_2 , C_1 and C_0 . The more significant counter section, which tracks the four stages of the 16-point FFT, will have only two bits, namely C_4 and C_3 . It is clear that in the first stage the coefficient address remains equal to '000' (only W^0) irrespective of the lower section counter value. The first stage is represented by the '00' combination of the higher section bits and hence the input channel of the multiplexer corresponding to this bit combination must always remain at '000'. In the second stage, the address '000' (W^0) is required for the first four computed butterflies and address '100' (W^4) is required for the next four butterflies. The second-stage '01' of the FFT is dependent on the status of the C_2 bit of the counter. This means that the second channel input should be set to 'C₂00'. The third stage '10' of the FFT requires the generation of four different addresses '000' (W^0), '010' (W^2), '100' (W^4) and '110' (W^6). It is clear that these addresses differ only in the C_2C_1 combination and C_0 remains equal to zero always. It means that the third channel of the multiplexer should be connected to 'C₂C₁0' to accomplish this task. The last stage '11' needs all the coefficients and hence the last channel must be connected directly to 'C₂C₁C₀'. The same technique can be very easily extended to any FFT size by following the formulations described earlier.

Simulation results: The new addressing scheme has been synthesised for different FFT lengths from the register-transfer level (RTL) Verilog description using Cadence *BuildGates* with 0.35μ Alcatel MTC 45000 complementary-metal-oxide-semiconductor (CMOS) technology library. The power based gate level simulations were carried out at a clock frequency of 100 MHz and at a supply voltage of 3.3 V and for one million clock cycles using Synopsys *DesignPower*. The same procedure was followed for the Cohen approach and the comparative results in terms of area and power for the different FFT lengths are shown in Tables 1 and 2, respectively. The power consumption, shown in Table 2, is the average power consumed by the respective circuit per clock cycle. It is clear from Tables 1 and 2 that our approach results in power and area savings in the range of 80 to 90% compared to the Cohen approach for the whole spectrum of FFT lengths. In Table 1, the area is slightly smaller for the coefficient address generation logic for a 2K-point FFT compared to 1K-point in a Cohen approach due to the optimisation of the subtractor with one fixed input by the synthesis tool. It is evident from Table 2 that the power consumption of the coefficient address logic depends on the switching activity of the inputs and outputs and not on the FFT size. The delay through our logic is only 1.13 ns

whereas the Cohen approach has a delay of 9.88 ns under identical input/output load conditions. This implies that our logic can operate up to a frequency of 885 MHz whereas the Cohen logic is limited to 101 MHz.

Table 1: Comparison of the two approaches in terms of area

FFT size	Cohen scheme [n]	Our scheme [n]	Reduction in area
			%
64	47	10	79
128	82	12	85
256	81	14	83
512	115	19	84
1K	126	21	83
2K	161	23	86
4K	158	25	84
8K	226	29	87

[n] equals number of equivalent NAND gates

Table 2: Comparison of the two approaches in terms of power

FFT size	Cohen scheme	Our scheme	Reduction in power
	μW	μW	%
64	125.0	26.9	78
128	143.0	23.5	84
256	112.0	21.5	81
512	107.9	20.0	81
1K	135.2	18.37	86
2K	172.2	18.24	89
4K	135.2	16.96	87
8K	105.0	17.94	83

Conclusion: We have presented a novel coefficient addressing scheme that is faster, more power and area efficient than existing approaches. The scheme will lead to the design of faster and more power and area efficient systems with embedded FFT processors.

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Gamma-ray induced pulsewidth broadening and power loss in modelocked Er-doped fibre laser

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A modelocked erbium-doped fibre laser (EDFL) exhibited a 9.7% decrease in its pump laser output power and pulsewidth broadening from 9.2 to 300 ps following a 10.14 kGy(Si) gamma-ray irradiation. A decrease in the EDFL intra-cavity power from the combined effects of the pump laser degradation, and colour centre induced absorption in the fibre segments and other EDFL components was responsible for the broadening and long recovery times required for restoration of modelocking.

Introduction: Radiation studies have been performed recently on erbium-doped fibre amplifiers (EDFAs) that are being introduced into transoceanic transmission systems [1, 2]. Studies regarding the dopants in EDFAs have determined that not all Er-doped fibres are created equal and that the dopants play a large role in the ability of the fibre to recover following irradiation [2 - 6]. Gamma-ray irradiations reported to date have ranged to 10^4 Gy(Si) while the data reported herein is reported for 10^4 Gy(Si), a dose of interest for some space applications.

Er-doped fibre-based devices may soon find applications in space such as high bit rate optical communication systems and photonic analogue-to-digital converters (ADCs). The rapid advancement in digital signal processing systems has led to an increased interest in the direct digitisation of high-frequency analogue signals. An ideal digital receiver is simultaneously capable of high sampling speeds and high resolution and does not require any signal down conversion. This can only be realised if rapid advancement occurs in ADC technology. The potential high bandwidth, reduced weight, and reduced power requirements makes photonics an attractive technology for wideband signal conversion. It is anticipated that photonic converters will be able to operate at sampling rates greater than 10 GS/s combined with extremely high resolution of the order of 12 to 14 bits. The erbium-doped fibre laser (EDFL) is a key component in a photonic ADC. In this Letter we characterise a passively modelocked EDFL, and irradiate the complete laser including its pump source, lenses and saturable absorber by gamma-rays to a total dose of 10.14 kGy(Si).

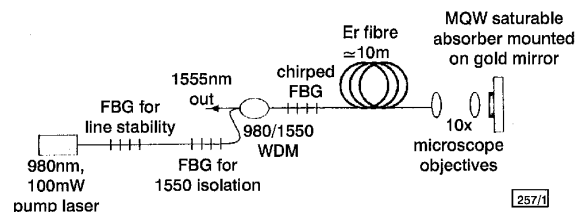


Fig. 1 Schematic diagram of laser components that were irradiated

Experiment: The experimental setup of the linear cavity EDFL passively modelocked by a multiple quantum well (MQW) semiconductor saturable absorber is shown in Fig. 1. The saturable absorber forms one end of the cavity with the other end formed by a chirped fibre Bragg grating. The laser was pumped at 980 nm through the chirped Bragg grating. The saturable absorber was grown by molecular beam epitaxy and consisted of 75 periods of alternating layers of 100 Å $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ quantum wells and 100 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barriers grown lattice matched on a semi-insulating InP substrate. This region encompassed a total thickness of only 1.5 μm . The InP substrate was thinned to approximately 50 μm and then coated with gold. This simple technique formed a high reflectivity nonlinear mirror in the laser cavity. The fibre laser cavity consisted of 10 m of AT&T HE980 erbium-doped fibre which had a measured dispersion value of 60 ps/nm/km. A 0.25 m length of standard singlemode fibre was spliced to the erbium-doped fibre which increased the cavity length to 10.25 m. The resulting cavity length corresponded to a fundamental repetition rate of 9.8 MHz. A 980/1550 nm wavelength division multiplexer (WDM) coupled the pump laser into the laser cavity. The dispersion compensating chirped fibre Bragg grating was centred at 1554.7 nm with a reflectivity of 96% and a bandwidth of 5.4 nm and is used as the output coupler. A free-space optical section consisting of two microscope objectives coupled the fibre to the saturable absorber. This setup had an optimum coupling efficiency of approximately 30%. A uniform high reflectivity fibre Bragg centred at 1555 nm was used to ensure that no modelocked pulses leaked back into the pump laser.

Prior to irradiation the Gaussian pulsewidth was calculated to be 9.2 ps with a corresponding spectral width of 0.54 nm. The pulse was not of soliton nature due to imperfect dispersion compensation. The EDFL system was exposed to Co_{60} gamma-rays in a continuous mode at an average gamma-ray dose rate of $D_{\gamma} \approx 13$ Gy(Si)/min. The irradiation was conducted for a total of 13 h resulting in a total gamma-ray dose of $D_{\gamma} = 10.14$ kGy(Si). The laser was powered up approximately 152 h following the irradiation.