

Low power receiver architectures for multi-carrier CDMA

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Abstract: The implementation of multi-carrier code division multiple access (MC-CDMA) receivers in digital hardware is considered. A low power algorithm is proposed which treats the received signal as a block of symbols, rather than processing the symbols individually. This reduces power by holding one input to the multiplier circuits used in the multi-carrier combiner multiplication constant for a number of clock cycles. This produces a 50% reduction in power consumption for a multi-user detection combiner circuit. This algorithm is also extended to the fast Fourier transform (FFT) block and allows an overall power drain reduction of 13% for the whole receiver. A software configurable version of the circuit, which allows a trade-off between power reduction and processing delay, is also described.

1 Introduction

Combining the advantages of OFDM (orthogonal frequency division multiplexing) and CDMA (code division multiple access) to realise multi-carrier CDMA [1, 2] provides a spectrally efficient spread spectrum multiple access technology, which may be incorporated into future mobile wireless systems. Since the terminals will be mobile, the power consumption of the terminals is an extremely important issue. Thus implementation aspects of MC-CDMA receivers and their impact on power consumption are investigated.

Multi-carrier CDMA is generally implemented using frequency domain processing as this allows low complexity multi-user detection algorithms to be utilised [3–8]. Time domain processing, where it is treated as a special case of direct sequence CDMA, has also been proposed [9], but is not considered here. A frequency domain processing multi-carrier CDMA receiver contains two main system blocks: an FFT block to demodulate the OFDM signals and a multi-carrier combiner block which equalises the signal and separates out the signals from the coded users. The combiner can employ a variety of techniques, applying simple rake filtering (MRC - maximal ratio combining), decorrelating or MMSE (minimum mean square error) multi-user detection to isolate the desired user's signal.

This paper will deal with receiver power consumption in two areas. Initially only the consumption in the combiner area will be considered neglecting the FFT block implementation. The minimisation of power consumption of the FFT has been the subject of numerous papers [10–13], and many of these techniques could be applied directly in a multi-carrier CDMA receiver. Analysis of the performance of the combiner block in isolation will be presented, and comparison between a conventional multiply-accumulate

(MAC) architecture and a novel low power algorithm for the combiner circuit will be shown. This low power approach will then be extended to include the FFT circuit and the other components of the receiver. A flexible approach allowing software reconfiguration of the power consumption of the circuit is also investigated, providing a single circuit which can trade off power usage for latency, depending on the user's requirements.

2 Multi-carrier CDMA

The multi-carrier CDMA systems considered in this paper use one code chip per carrier and should not be confused with direct sequence CDMA systems transmitted on multiple carriers [14]. The signal is spread before being converted into a parallel data stream which is then transmitted over multiple carriers. If the processing gain is equal to the number of carriers then this system modulates all the carriers with the same data bit, but with a phase shift on each carrier determined by the spreading code as shown in Fig. 1. This multi-carrier modulation can also be implemented using an inverse FFT.

A BPSK system is considered. If the k th chip of the spreading code for user u is defined as $c(k, u) \in \{-1, +1\}$ then the transmitted baseband signal for m th data symbol $b(m)$ is

$$x(n) = \sum_{k=0}^{N-1} \exp(j2\pi kn/N) c(k, u) b(m) \quad (1)$$

To overcome the effect of inter-symbol interference, this baseband signal is cyclically extended by more than the channel delay spread, to allow transmission of an interference free symbol. The full structure of an MC-CDMA transmitter is shown in Fig. 2. By using a guard interval, the receiver selects the portion of the signal that is free from inter-symbol interference. This is processed by an FFT block to demodulate the multiple carriers.

The effect of a multipath channel $h(n)$ at the output of the FFT is narrowband for each carrier, $H(k)$, and therefore the equalisation and despreading can be incorporated in a single combining operation to estimate the transmitted data bit. If the output of the FFT block at frequency bin k is

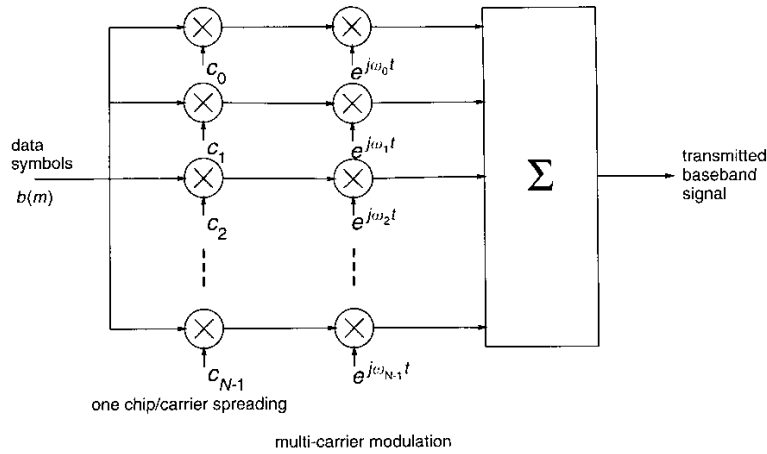


Fig. 1 One chip per carrier multi-carrier CDMA

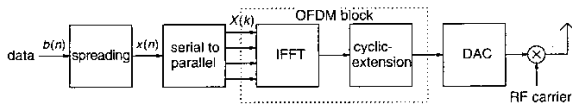


Fig. 2 Multi-carrier CDMA transmitter

defined as $Y(k)$ then the combining operation and hard decision operation can be represented by:

$$\hat{b}(n) = \text{sign} \left\{ \sum_{k=0}^{N-1} \Re \{ c(k, u) A(k) Y(k) \} \right\} \quad (2)$$

The entire receiver structure is shown in Fig. 3.

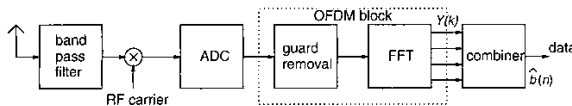


Fig. 3 Multi-carrier CDMA receiver

The equaliser coefficient $A(k)$ can be used to implement a frequency domain rake filter if it is set to match the channel: $A(k) = H^*(k)$ [1, 6]. Linear multi-user detection can also be implemented by simply changing the coefficient $A(k)$. A decorrelator can be obtained with $A(k) = H^*(k)/|H(k)|^2$ and the MMSE solution can be implemented using

$$A(k) = H^*(k)/(|H(k)|^2 + \lambda) \quad (3)$$

where λ is a parameter dependent on the receiver signal to noise ratio and the number of users [4].

The implementation of this combiner, for an N carrier system, can be achieved using a MAC unit as shown in Fig. 4. In this architecture, the output of the FFT and the equaliser coefficients ($A(k)$) are buffered and a serial MAC is performed to obtain the data bit estimate. Since the code chips can only be $+1$ or -1 , the multiplication by these chips is achieved by changing the sign of the product as required.

Fig. 5 shows a flowchart describing the operation of this combiner circuit including the calculation of equaliser coefficients. It is assumed that a pilot symbol used for channel estimation is sent every M symbols.

3 Low power combiner architecture

The power consumption of a circuit can be reduced significantly by reducing the amount of switched capacitance. In the MAC based architecture of Fig. 4, both inputs to the multiplier are switched every clock cycle as new input data samples and equaliser coefficients are multiplied. Since the multiplier is the largest component in the circuit, reducing the amount of switching here should have a major effect on its power consumption.

A block based approach [15] has previously provided an effective method for producing a low power discrete cosine transform. In the case of an MC-CDMA receiver, a similar approach can be applied, if it is assumed that the channel fading is sufficiently slow that it allows the retention of the same channel equalisation coefficient for a significant block length. The channel fading due to motion at pedestrian speeds is sufficiently slow to apply this approach, although at vehicular speeds problems may be encountered.

Under these conditions, a block of data containing M symbols can be buffered. The data are then processed, one carrier at a time for the entire block length of symbols. A block of memory is used to store the accumulated total for each symbol, and the most significant bit (MSB) of each word provides the data estimate for each symbol. Fig. 6 shows the architecture for this circuit. This circuit requires a larger memory buffer to store the FFT outputs for M symbols.

The detailed operation of this architecture is shown in the flowchart in Fig. 7. The principal result of this architecture is that the equaliser coefficient and the CDMA code are held constant for M clock cycles (the inner loops of the flowchart), therefore one input to the multiplier is switched at a much lower frequency and hence the resulting power consumption should be significantly lower.

3.1 Power analysis

To evaluate the power consumption of the proposed architecture, both the MAC based combiner and the low power block based combiner were synthesised using Ambit Buildgates [16] and the Alcatel 0.35 μ library. A 64 carrier system was assumed and the data were divided into blocks of 32 symbols, with the first symbol in the block being used as a pilot for channel estimation. A word length of 16 bits was assumed for the output data from the FFT block. The default 16-bit multiplier from the library was implemented. Additional circuitry was included to estimate the channel

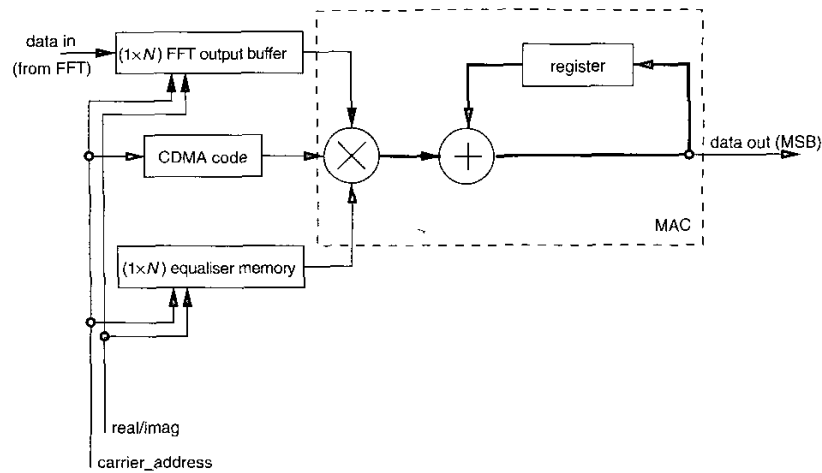


Fig. 4 Combiner incorporating multiply accumulate circuit

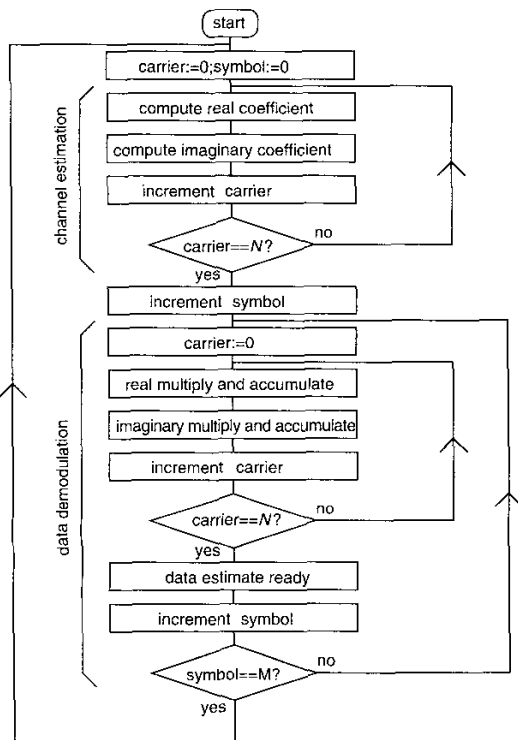


Fig. 5 Flowchart for combiner incorporating multiply accumulate circuit

coefficients, including a division circuit. These do not increase the power consumption significantly as they are only used for 1 out of every 32 symbols.

Power analysis was performed on the synthesised model using Synopsis Design Power [17] assuming a clock rate of 10 MHz and data symbol rate of 156 kHz. This analysis was restricted to measuring the dynamic power consumption due to switching. Simulations were performed using a single user scenario and scenarios with additional interfering users modelling typical performance of the system.

Random CDMA codes were generated for the pilot symbols and for one user. The data for the single user scenario were generated by spreading known pilot symbols and random binary data symbols by CDMA codes. The spread symbols were multiplied by complex Gaussian

random variables to model the effect of passing through parallel Rayleigh fading narrowband channels, and give the appropriate value for the FFT output at the receiver. No explicit Gaussian additive noise was added, and the noise variance parameter in the MMSE equaliser, λ , was set arbitrarily to the value of 1. For the scenarios with up to 15 interfering users, complex Gaussian distributed noise was added to the signal at the power level which would be caused by that number of interfering users.

The switched power consumption for both circuits is shown in Table 1 for the single user and 15 interfering user case (16 users). It is clear that the block architecture significantly reduces the power consumed in both cases to a level that is approximately half that of the MAC based architecture. This power reduction is achieved because one of the multiplier inputs is switched at a negligible rate compared to the other input. This power reduction occurs in both the memory blocks and in the multiply and accumulation circuits, in about equal amounts. A comparison of the power consumption of the circuits is shown in Fig. 8 for all scenarios with 1 to 16 users. This indicates that the reduction in power consumption is independent of the level of interference, and that the block based architecture approximately halves the power used in all cases.

4 MC-CDMA receiver architecture

To implement a MC-CDMA receiver requires three algorithmic blocks: guard interval removal, FFT and the combiner. However, these need not be implemented individually. The guard interval removal is merely the selection of the ISI free part of the received signal and therefore this can be implemented very simply by controlling when the signal is sampled. The FFT and the combiner both involve multiplications and additions and therefore it is possible to implement both using the same hardware with appropriate control signals.

Fig. 9 shows the overall architecture of the circuit. It contains four memory blocks, a control unit, an arithmetic unit and an interface to the analogue receiver. Two of the memory blocks are interchangeable buffers, one is used to store the incoming signal, which is sampled at a rate much lower than the processing clock rate, and the other is used as the workspace for the FFT operation. These blocks are interchanged when the processing of the FFT is finished and enough samples to start again are in the other buffer. The other memories are used to store the equaliser

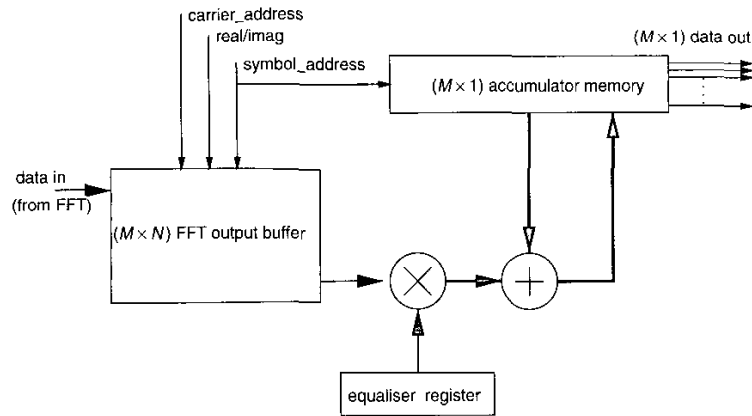


Fig. 6 Low power block based combiner

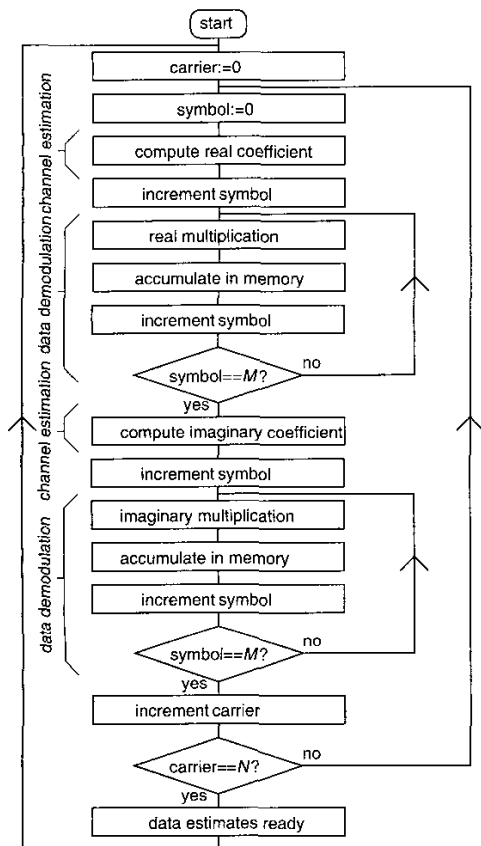


Fig. 7 Flowchart for low power block based combiner

coefficients and to sum the totals produced by the combiner operation. The arithmetic unit provides the multipliers required for both the FFT and combining algorithms as well as a divider to compute the MMSE equaliser coefficients, see (3).

The reconfigurable power consumption is provided by implementing a flexible length block algorithm. In the circuit the granularity of processing can be varied to achieve the desired balance between power consumption and minimising the delay in the data. The data are divided into blocks of M data bits. This requires memory buffers of size NM complex elements, where N is the size of the FFT.

The highest power, lowest latency mode operates when $M = 1$. In this case the data bits are processed one at a time.

Table 1: Comparison of MAC based and block based architectures

Architecture	MAC		Block	
No. users	1	16	1	16
Power usage in circuits in mW				
Memory	13.1	12.9	6.2	6.2
MAC	11.8	11.3	—	—
Multiply	—	—	1.8	2.2
Add	—	—	3.8	4.4
Other	1.9	1.7	1.2	1.1
Total	26.8	25.9	13.0	13.9

The received signal is buffered in sections of N samples (in bit reversed order). When one section is buffered, the memory buffers are swapped and the FFT operation is then performed on the N -point memory through $\log_2 N$ stages, with the results overwriting the data. To allow an easier implementation of a low power block based algorithm, the butterfly operations of the FFT are performed using two multipliers, achieving the four multiplications required in two clock cycles. Otherwise the FFT operates sequentially, completing each stage in N clock cycles. The combiner stage also uses the two multipliers performing its $2N$ multiplications in N clock cycles.

When switching to a lower power mode, data are buffered in blocks containing M data bits. The sampled data are stored in sections of MN samples, with the least significant address bits reverse ordered in preparation for the FFT. The FFT is then performed in block fashion on the M data bits. Each butterfly operation is performed sequentially on the equivalent array elements for each successive data bit. This keeps one input of the multipliers (the FFT coefficients) fixed for at least M clock cycles. This block based approach is also applied to the combiner multiplication where the equaliser coefficients are held constant for M cycles and the combined sums are stored in the accumulator memory. When decoding is complete, the resulting data estimates can be read out of accumulator memory.

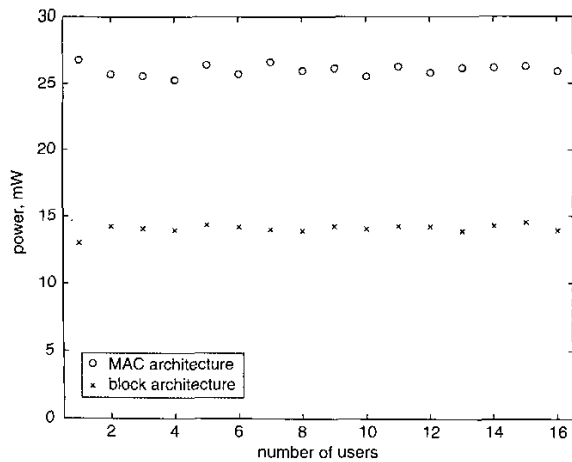


Fig. 8 Comparison of power consumption for varying numbers of users

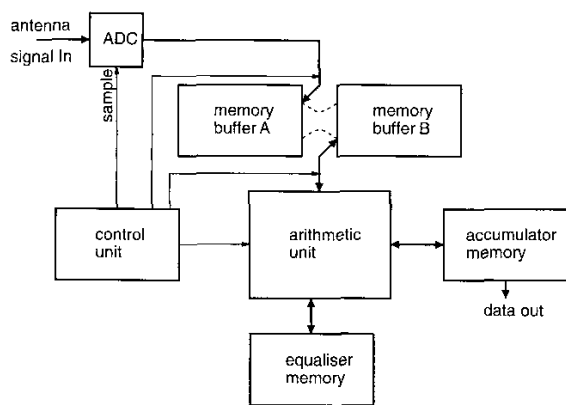


Fig. 9 Receiver circuit block diagram

The power reduction here will be less than the 50% obtained when the combiner circuit is implemented alone. The reason is that the FFT coefficients are not always switched every clock cycle even when $M = 1$. The rate of change depends on which stage of the FFT is being processed, and at earlier stages the coefficient changes slowly; however, at the last stage, the coefficient is switched at the clock rate and therefore significant power saving is made here.

Fig. 10 shows the algorithm used by the FFT-combiner circuitry. Note that W^k represents the FFT coefficient $\exp(-j2\pi k/2^{\text{stage}})$. The inner loops where one of the

multiplier inputs is held constant are shaded. In the combiner phase of the algorithm this is for M clock cycles, but in the FFT phase of the algorithm the length of time one of the inputs is held constant depends on the stage of the FFT being processed.

The same circuitry can be used for both the FFT and combining operations. Fig. 11 shows the two-multiplier circuit configured for performing an FFT butterfly operation. This takes three cycles to complete, although the processing of the next pair of data points can begin after two cycles. In the first cycle the first data value ($Y(i + 2^{\text{stage}-1})$) is input and buffered (in R1), with the multipliers used to compute the real part of the product ($W^k Y(i + 2^{\text{stage}-1})$) which is buffered (in R3). In the second clock cycle, the imaginary part of the product is computed and the second data value ($Y(i)$) is read in and buffered (in R2). The real and imaginary products are subtracted from the second data value input to produce the first output value ($Y(i) - W^k Y(i + 2^{\text{stage}-1})$). In the third clock cycle, using the buffered values the sum $Y(i) + W^k Y(i + 2^{\text{stage}-1})$ is produced. Simultaneously the first cycle processing for the next two data points occurs.

The two multipliers are also used in the combiner as shown in Fig. 12. Here the algorithms is much simpler with the real and imaginary multiplications performed in parallel and the code multiplication achieved by either adding or subtracting the sum of the products to the accumulated total in memory.

The algorithm also includes a channel estimation phase, where pilot symbols are transmitted to allow the receiver to estimate the channel. The channel estimation processing occurs after the FFT in place of the combiner algorithm. To estimate the MMSE coefficients from the channel estimates an additional division circuit is required. This does not have a significant effect on the power consumption as it is only used during the channel estimation phase, which is only $\sim 3\%$ of the time used for combiner operations.

4.1 Power analysis

The circuit was synthesised using the Alcatel 0.35 micron library [18]. The bit resolution for the multipliers, divider and memory buffers was 8-bit. Fixed point FFT simulations with an average normalised signal power of 32^2 , and 6-bit FFT coefficient values, indicated that a quantisation noise level of -18 dB relative to the signal power is produced and this should not have a significant impact on the combining algorithm. The accumulator memory and associated addition circuit were 16-bit.

A 64-carrier MC-CDMA system was implemented, requiring a 6-stage FFT. A cyclic extension of 16 samples was assumed giving a total symbol length of 80 symbols. To

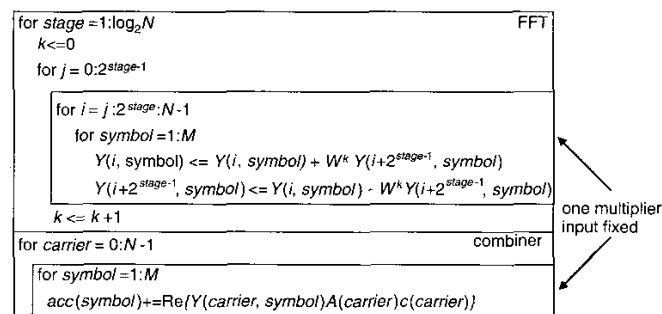


Fig. 10 Algorithm for FFT and combiner operation

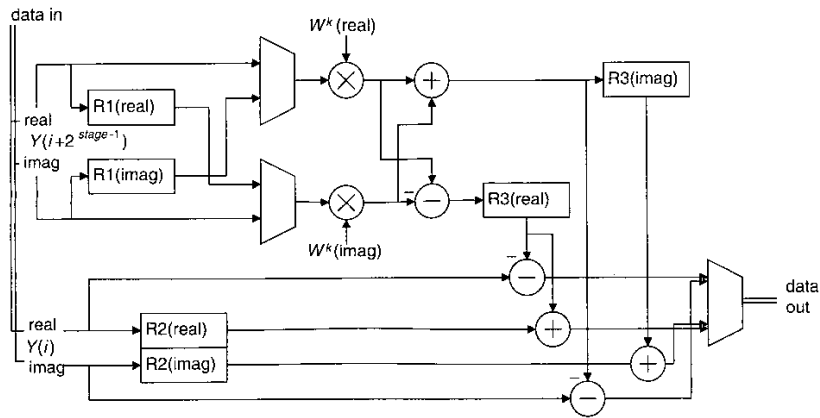


Fig. 11 Two-multiplier circuit configured as FFT

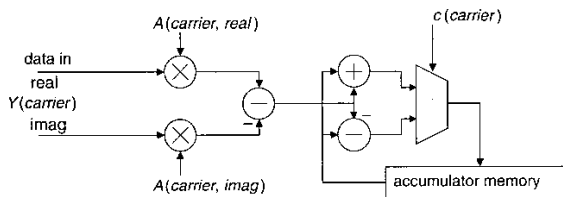


Fig. 12 Two-multiplier circuit configured as combiner

allow time to perform the FFT, the circuit was clocked at eight times the sample rate. A clock rate of 20 MHz could be achieved comfortably, resulting in a sample rate of 2.5 MHz and underlying symbol rate of 31.25kHz. Block lengths (M) were varied from 1 up to 32 symbols, giving processing delays from 32 μ s up to 1ms. In these simulations, only the power consumed in the arithmetic and control units was measured, and the power consumed by the memory neglected, firstly because a number of different low power memory strategies could be used but a full investigation of these is beyond the scope of this paper, and secondly to reduce simulation time and circuit size.

Table 2 shows the effect on power consumed of varying the block length. The data used for these simulations assumed one user transmitting across a Rayleigh fading channel with average receiver E_b/N_0 of 10 dB. It is quite clear from the simulations that a latency/power trade-off can be achieved. At a cost of a 1ms processing delay, a 13% reduction in power is achieved.

Table 2: Comparison of power consumption with block length

Block length, M	Latency, μ s	Power, mW
1	32	18.8
2	64	18.4
4	128	17.8
8	256	17.3
16	512	16.9
32	1024	16.3

This appears poor compared to the 50% power reduction, which can be achieved in the combiner circuit alone; however, the combiner circuit only accounts for 8% of all multiplications and therefore 4% of the power reduction can be attributed to this reduction. The other 9%

of power reduction therefore occurs in the FFT, giving an average 10% power reduction across the whole FFT. This is likely to be mainly in the last stages of the FFT where the coefficients are switched at a high rate. The block algorithm has little effect on the earlier stages.

5 Conclusions

This paper has discussed important implementation issues associated with multi-carrier CDMA mobile wireless receivers – in particular the use of a block based processing algorithm to reduce power consumption. By processing multiple symbols as a block, one of the inputs to the multipliers used for the FFT and combining operations is held constant for a number of clock cycles, reducing switching and hence power consumption. This approach allows almost a 50% reduction in the power consumed by the combiner sub-circuit. The algorithm can also be extended to the FFT algorithm required. Here the power reductions are smaller, but some reduction is still achieved. The cost of using a block based algorithm is a small increase in data latency of about 1ms/32 data symbols. It is possible to design a software configurable architecture which can select the lowest power block size when latency is not a problem, but uses a higher power algorithm to provide a real time response if required.

6 Acknowledgment

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