

A Low Power Heterogenous Reconfigurable Architecture For Embedded Generic Finite State Machines

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ABSTRACT

Domain-specific reconfigurable arrays are usually designed for specific applications and provide a good compromise between speed, power and flexibility. In this paper, a novel reconfigurable Finite State Machine (FSM) array is presented for implementing generic FSMs. Compared with commercial FPGA devices, the new architecture provides the following reductions: up to 90% in power consumption, up to 55% in area and around 20% in delay time.

I. INTRODUCTION

Reconfigurable System-on-Chip (SoC) technology emerged to satisfy demands for both flexibility and efficiency. A domain-specific reconfigurable array for generic FSM is presented in this paper. The core is written in RTL hardware description language and synthesized with mainstream CAD tools with standard cell.

In [1] and [2], two special reconfigurable systems are described. One is designed specifically for real-time image processing. Another one is built for heavy load application such as MPEG2 encoding, DNA string comparison and so on. Numerous works have been done on reconfigurable architecture and their implementation. Unfortunately no architecture is designed specifically to meet both low power consumption and reconfigurability for FSMs.

Our architecture is described in section 2. The power saving approaches adopted in the design are introduced in section 3. Finally, the experimental results and summary are presented in the section 4 and 5.

II. RECONFIGURABLE FSM ARCHITECTURE

The proposed architecture can be divided into two functional sections: logic and sequential, as shown in Figure 1. The sequential block and logic

block are the functional units in their respective sections. Each functional unit is made up of product-term blocks (PTBs) [3].

The function of the sequential section is to implement transition between the current state and the next state. The function of the logic block is to realize some combinational Boolean functions. PTB acts as basic computing unit to realize some basic Boolean functions. The input signals are up to 8 in the current design and can reach both sections through routing resources. The outputs of the sequential blocks can be routed to logic blocks and also feedback to other sequential blocks. The number of logic blocks depends on the number of FSM's outputs. The 8 sequential blocks in the current design can implement an FSM with a maximum of 256 (2^8) states.

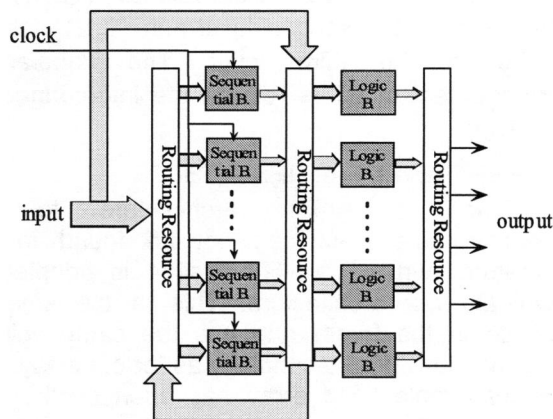


Figure 1: The reconfigurable FSM architecture

III. LOW POWER IMPLEMENTATION

The most popular routing network is balanced symmetrical construction. Functional modules are equally placed in a relatively smooth sea of routing resources which is made up of switch boxes and connection blocks. The mass of routing resources bring to the system powerful flexibility, but pay out the cost of high area and power consumption.

Our unbalanced architecture uses large sections with fixed inter-connection blocks to replace flexible switch boxes in order to reduce power consumption and area. There are three internal connection levels. In the first level, multiplexer based switch boxes are used to feed the inputs of logic computing modules. In this level, internal connects keep their flexibility to make sure that input signals can reach their destination. In the second and third interconnection levels, most of the interconnects are made up of fixed connection which can greatly reduce power consumption and area compared to using switch boxes. The routing network area is reduced at the cost of flexibility. So, some redundant computing units are employed to compensate for the inconvenience of internal data exchange.

A two-input reconfigurable logic computing unit is adopted to implement an AND sub-module or an OR sub-module. The reason for using an unbalanced architecture is to select different size PTBs in different levels.

We refer to the size of a PTB using tuple (i, p, o) where i is the number of inputs, o is the number of outputs, and p is the number of product terms. From the experimental data in [4], $(16,4,1)$ is selected for the PTBs in the first level, $(2,1,1)$ for the PTBs in the second level and $(4,1,1)$ for the PTBs in the third level. The unbalanced arrangement of PTBs reflects the interconnection mapping.

IV. EXPERIMENTAL RESULTS

Since a similar architecture to our reconfigurable FSM can not be found in the literature, Virtex-E xcv50e-6cs144 is adopted to evaluate our architecture. This is the smallest device in the family and has the same voltage supply and CMOS technology as for our array. Our reconfigurable FSM array has been synthesized with from Cadence Ambit BuildGates using the UMC 0.18um standard CMOS cell library. Several commonly used test cases from LGSynth93 [5] have been implemented on both FPGA device and our array.

The power consumption and area for our architecture and FPGA are shown in Figures 2 and 3. Our architecture achieves saving from 74% to 90% in power and from 38% to 55% in area. Because the amount of fixed lines adopted, the flexibility of our architecture is reduced. This makes the critical path similar for the different cases. The average delay time of all tested cases is 20% shorter than FPGA.

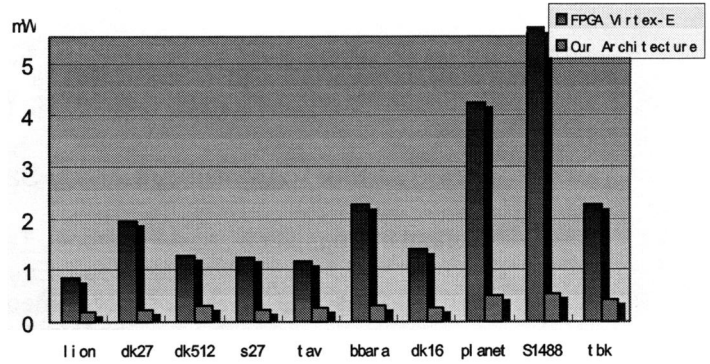


Figure 2: Experimental Results for Power Consumption

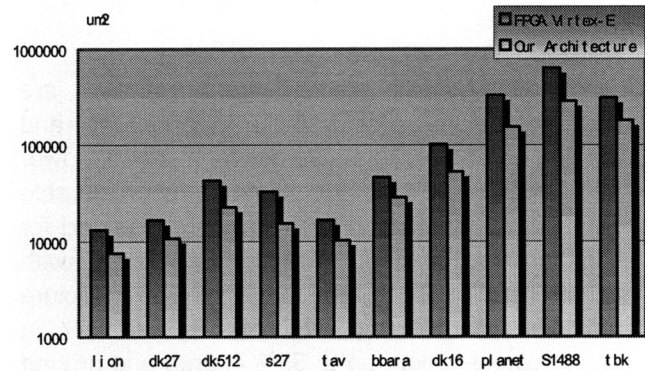


Figure 3: Experimental Results for Area and Delay

V. SUMMARY

A novel reconfigurable low-power domain-specific architecture for FSM-based control circuits was introduced in this paper. Compared to commercial FPGAs, our design is able to obtain on average a reduction of 82% in power consumption, 44% in area occupation and 20% in delay. These figures show that the proposed reconfigurable array architecture provides an efficient hardware platform for the implementation of generic FSMs in various power sensitive designs.

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