

# Dual low-power and crosstalk immune encoding scheme for on-chip data buses

Z. Khan, A.T. Erdogan and T. Arslan

A new encoding scheme is introduced for low-power and crosstalk immune communication of generic data on long parallel on-chip buses. The scheme uses a limited weight codebook with one-to-one data-to-code mapping. The new scheme and its implementation using a generic system-on-chip platform are described and results are provided that indicate a 30% saving in total switching activity with an 8-bit communication example.

**Introduction:** The scaling of CMOS technology to ultra-deep sub-micrometre causes the coupled switched capacitance to dominate the wire-to-substrate capacitance. This coupled capacitance in turn will lead to crosstalk noise, which is a potential source for delay faults, logical malfunctions and energy consumption in on-chip communication. Techniques based on bus invert [1] and the coupling driven bus invert (CBI) [2] are among those commonly used in the literature for reducing self and coupled switched capacitance for generic data of unknown probabilistic information. However, none of the techniques in the literature is capable of both eliminating worst crosstalk coupling and reducing power for such data. Worst crosstalk coupling is classified into three types namely type-4, type-3 and type-2 [4]. In type-4, three adjacent wires undergo opposite state transition (e.g. 101-to-010). In type-3, two adjacent wires undergo opposite state transition while the third maintains its previous state (e.g. 101-to-110) and in type-2, the centre wire is in opposite state transition with one adjacent wire while the other adjacent wire undergoes the same transition as the centre wire (e.g. 001-to-110). The coupled switched capacitance becomes  $4 * C_f$ ,  $3 * C_f$  and  $2 * C_f$  in type-4, type-3 and type-2 crosstalk, respectively, with  $C_f$  being the coupled capacitance when only one wire changes state (type-1 crosstalk). The method proposed here eliminates worst crosstalk coupling and reduces self transitions for generic data in which probabilistic information cannot be known *a priori*.

**Method description and implementation:** Spatially redundant limited weight code (LWC) has Hamming weight less than the data it represents and is used in off-chip communication for energy efficiency [3]. The concept of the limited weight code can be exploited for the case of on-chip communication to achieve two performance goals. The first is worst crosstalk coupling elimination and the second is energy efficiency. The flow graph of the codec scheme is shown in Fig. 1. The encoder performs the encoding in three stages. The first stage performs modulo-2 addition of the present and previous raw  $m$ -bit data ( $y_m(n) = x_m(n) \oplus x_m(n-1)$ ). The second stage maps the  $m$ -bit pattern with a  $p$ -bit LWC, i.e. ( $L_p(n) = m/2$ -LWCCodebook( $y_m(n)$ )). This stage consists of a semi-perfect  $m/2$ -limited weight codebook of size  $2^m \times p$  bits. The codebook has been developed with emphasis to eliminate the worst crosstalk coupling. The organisation of the  $p$ -bit limited weight codewords is done in such a way that if two codewords of Hamming weight greater than zero are summed up using modulo-2 addition, the resulting pattern eliminates type-4, type-3 and type-2 crosstalk coupling discussed in [4] with a modest increase in type-1 crosstalk. However, type-1 is the least severe crosstalk coupling. The modulo-2 addition is performed in the third stage on the pattern already present on the bus ( $D_p(n-1)$ ) and the corresponding codeword  $L_p(n)$  to be transmitted on the bus ( $D_p(n) = L_p(n) \oplus D_p(n-1)$ ). The resulting pattern  $D_p(n)$  from the modulo-2 adder not only is immune to worst crosstalk coupling (type-4, type-3 and type-2) but also has less self switching activity. An  $m$ -to- $p$ -bit expansion in the on-chip data bus occurs.

The decoder is exactly a reverse replica of its encoder. In the first stage, present and previous bus states are modulo-2 summed up to recover the  $p$ -bit codeword  $L_p(n)$ , i.e.  $L_p(n) = D_p(n) \oplus D_p(n-1)$ . The codeword is then applied to the  $m$ -bit LWC decodebook and the  $m$ -bit data pattern  $y_m(n)$  is recovered ( $y_m(n) = m$ -bitLWCDcodebook( $L_p(n)$ )). This  $m$ -bit pattern is the result of the modulo-2 addition of the present and previous original  $m$ -bit data. The third stage then recovers the original  $m$ -bit raw data by performing modulo-2 addition of the present  $m$ -bit pattern  $y_m(n)$  and the previous  $m$ -bit raw data  $x_m(n-1)$ , i.e.  $x_m(n) = y_m(n) \oplus x_m(n-1)$ . The bandwidth  $m$  can be 4 or any integer

multiple of 4. For 8-bit transfer, the 8-bit bus is partitioned into two 4-bit lanes. Each lane is encoded and decoded according to the proposed method using a 4-to-6-bit codebook and a 6-to-4-bit decodebook. Inter-lane worst crosstalk coupling is eliminated by a shield wire between the lanes. The 8-bit bus expands to 13 bits. The codec architecture has been tested on AMBA-AHB based generic SoC platform. The target is the AHB data bus.

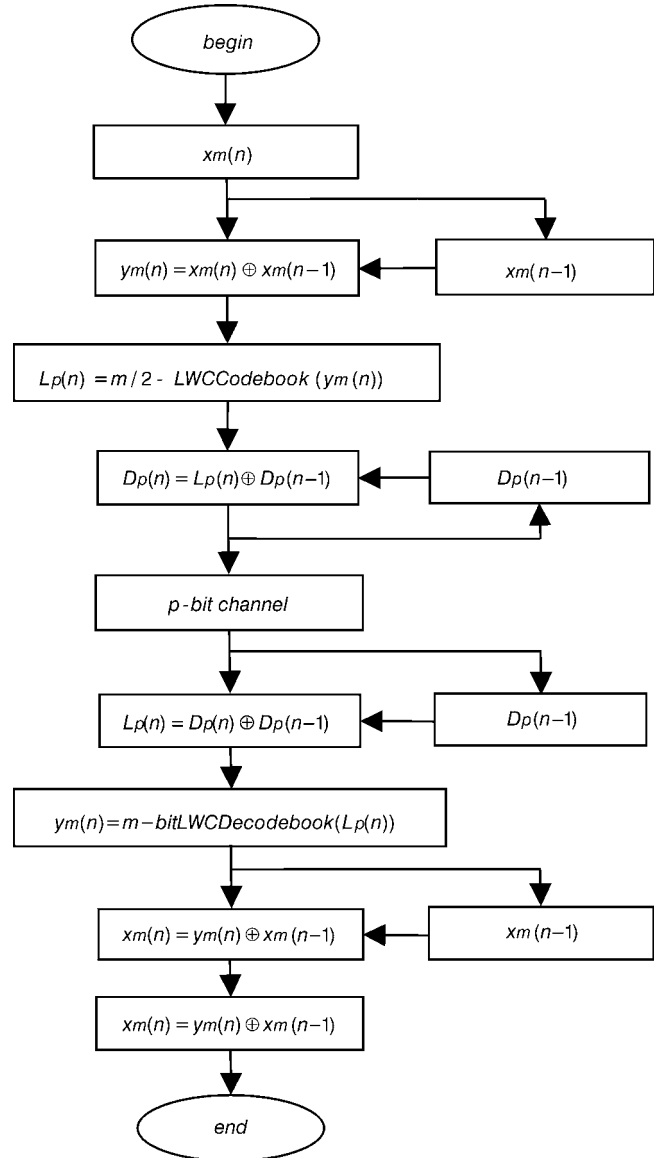


Fig. 1 Flow graph of the codec scheme

**Simulations and results:** The codec architecture has been synthesised down to 0.18  $\mu$ m CMOS technology. The resulting netlist is then simulated for an 8-bit biomedical data set. The 8-bit biomedical data is chosen as a sample example. Any data type of any transfer size can be chosen to prove the dual purpose of the encoding scheme. A test bench is developed to simulate the code of the AMBA-AHB bus and the proposed codec architecture using a Verilog-XL simulator. The number of self and coupled switched transitions is monitored at the output of the encoder. The total switching activity has been estimated using the approximate expression given below (1) that is derived using lumped model of the on-chip bus:

$$N_t = N_x + \lambda * (4 * N_4 + 3 * N_3 + 2 * N_2 + 1 * N_1) \quad (1)$$

where  $N_t$ ,  $N_x$ ,  $N_4$ ,  $N_3$ ,  $N_2$  and  $N_1$  are, respectively, total, self, type-4, type-3, type-2 and type-1 switching activity and  $\lambda = C_f/C_L$  is the ratio of coupling to wire-to-substrate capacitance and is 3.2 for 0.18  $\mu$ m CMOS technology and a minimum distance between wires. The results are shown in Table 1. The total switching as given by (1) has also been

calculated for raw input data, bus invert [1] and CBI [2] schemes for comparison with the proposed encoding scheme.

**Table 1:** Percentage reduction in total switching activity for 8-bit biomedical data set

Encoding scheme	Self switching	Type-4 coupling	Type-3 coupling	Type-2 coupling	Type-1 coupling	Total switching	% reduction
Raw input data	37 784	376	3281	192	22 017	145 777	0
Bus invert	22 584	331	3290	203	19 794	123 044	16
CBI	38 072	2587	1582	1578	19 845	159 976	-9
Proposed scheme	20 646	0	0	0	25 653	102 735	30

The simulation results indicate 45% and 30% reduction in self and total switching activity, respectively, while eliminating all types of worst crosstalk coupling. Similar results have been achieved for other data types and transfer sizes. The bus invert, on the other hand, produces a reduction of about 16% in total switching activity, whereas the CBI scheme proved to be more power consuming. The reason for this increase is that CBI depends on the total coupled switched capacitance in a particular data transfer and if an 8-bit data sample has less than eight total coupled switched transitions in a particular transfer, the CBI coder will not invert the data. The biomedical data is characterised by a high degree of correlation with minimum crosstalk coupling probability per data transfer. Out of the 14 642 samples, none of the data samples got inverted by the CBI coder. The decorrelation at the output of the CBI encoder caused an increase in the total switched capacitance for the biomedical data set. The proposed method proved to be more efficient than the bus invert and the coupling driven bus invert schemes regarding crosstalk delay elimination and reduction in total switching activity. The latency introduced by the Codec Architecture does not affect the performance of the AMBA-AHB bus and is therefore not discussed here.

*Conclusions:* A novel power saving as well as crosstalk immune encoding scheme for generic data of unknown probabilistic information has been presented. The method targets reduction of self and worst crosstalk coupled switched capacitance on long parallel on-chip data buses implemented in ultra-deep submicrometre SoC systems. Results have been presented for an 8-bit communication example indicating crosstalk delay elimination and 30% power efficiency of the encoding scheme. The method reduces the bit error probability and improves the reliability and robustness of the on-chip communication to a considerable extent, with only a small increase in bandwidth.

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### References

- 1 STAN, M.R., and BURLESON, W.P.: 'Bus-invert coding for low-power I/O', *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 1995, **3**, (1), pp. 49–58
- 2 KIM, K.-W., BAEK, K.H., SHANBHAG, N., LIU, C.L., and KANG, S.M.: 'Coupling-driven signal encoding scheme for low-power interface design'. *Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM Int. Conf.*, 5–9 November 2000, pp. 318–321
- 3 STAN, M.R., and BURLESON, W.P.: 'Coding a terminated bus for low power'. *VLSI, 1995. Proceedings, Fifth Great Lakes Symposium*, 16–18 March 1995, pp. 70–73
- 4 DUAN, C., TIRUMALA, A., and KHATRI, S.P.: 'Analysis and avoidance of crosstalk in on-chip buses', *Hot Interconnects*, 2001, **9**, pp. 133–138