A LOW POWER MMSE RECEIVER FOR MULTI-CARRIER CDMA

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ABSTRACT

The power consumption of a minimum mean square error (MMSE) multi-carrier CDMA receiver implemented in digital hardware is considered. A low power block based architecture is investigated for the combiner sub-system, and compared with a multiply accumulate circuit approach. Simulations using data consistent with typical performance of a multi-carrier CDMA receiver indicate that the block based approach can produce a power reduction of around 50%.

1. INTRODUCTION

Multi-Carrier CDMA [1, 2] is a spread spectrum technology which combines the advantages of OFDM (orthogonal frequency division multiplexing) and CDMA (code division multiple access) to produce a spectrally efficient multi-user radio access system. This radio access system may be utilized in future mobile wireless systems, and hence the power consumption of terminals is an issue.

Multi-carrier CDMA can be implemented using either time domain processing [3], where it is treated as a special case of direct sequence CDMA (but with non-bipolar codes), or using frequency domain processing. A frequency domain processing multi-carrier CDMA receiver contains two main system blocks, a FFT block to demodulate the OFDM signals and a combiner block which equalises the signal and separates out the coded users. The combiner can employ a variety of techniques applying simple RAKE filtering (MRC - maximal ratio combining), or decorrelating or even MMSE multi-user detection to isolate the users signal. This paper deals with an implementation of a receiver containing an MMSE combiner block. The minimisation of power consumption of the FFT has been the subject of numerous papers [4, 5, 6, 7], and many of these techniques could be applied in a multi-carrier CDMA receiver. Therefore only the minimization of the power in the combiner block is considered in detail in this paper.

2. MULTI-CARRIER CDMA

The multi-carrier CDMA considered in this paper uses one code chip per carrier and should not be confused with direct sequence CDMA systems transmitted on multiple carriers [8]. The signal is spread before being converted into a parallel data stream which is then transmitted over multiple carriers. If the processing gain is equal to the number of carriers then this system modulates all the carriers with the same data bit, but with a phase shift on each carrier determined by the spreading code. This is shown in figure 1. This multi-carrier modulation can also be implemented using an inverse FFT.

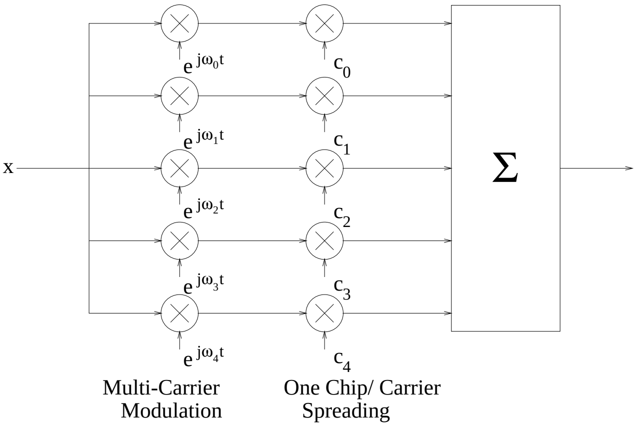

Figure 1: One Chip per Carrier Multi-Carrier CDMA

If the kth chip of the spreading code for user u is defined as $c(k,u) \in \{-1,+1\}$ then the transmitted baseband signal for mth data symbol $b(m)$ is:

$$x(n) = \sum_{n=0}^{N-1} \exp\left(j2\pi kn/N\right) c(k,u) b(m) \qquad (1)$$

To overcome the effect of inter-symbol interference, this baseband signal is cyclically extended by more than the channel delay spread, to allow transmission of an interference free symbol. The full structure of a MC-CDMA transmitter is shown in figure 2.

By using a guard interval, the receiver selects the portion of the signal that is free from inter-symbol interference. This is processed by an FFT block to demodulate the multiple carriers.

The channel effect of a multipath channel $h(n)$ at the output of the FFT is narrowband for each carrier, $H(k)$, and therefore the equalisation and despreading can be incorporated into a single combining operation to estimate the transmitted data bit. If the output of the FFT block at frequency bin k is defined as $Y(k)$ then the combining operation can be represented by:

$$\hat{x}(n) = \mathrm{sign}\{\sum_{k=0}^{N-1} \Re\{c(k,u)A(k)Y(k)\}\} \qquad (2)$$

The entire reciever structure is shown in figure 3.

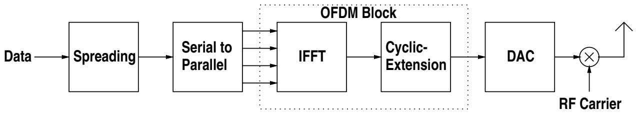

Figure 2: Multi-Carrier CDMA Transmitter

The equaliser coefficient $A(k)$ can be used to implement a frequency domain rake filter if it is set to match the channel: $A(k) = H^*(k)$. Linear multi-user detection can also be implemented by simply changing the coefficient $A(k)$. A decorrelator can be implemented by setting $A(k) = H^*(k)/|H(k)|^2$ and the MMSE solution can be implemented using $A(k) = H^*(k)/(|H(k)|^2 + \lambda)$ where λ is a parameter dependent upon the signal to noise level and the number of users.

The implementation of this combiner can be achieved using a multiply accumulate unit as shown in figure 4 for an N carrier system. In this architecture, the output of the FFT and the equaliser coefficients ($A(k)$) are buffered and a serial multiply accumulate performed to obtain the data bit estimate. Since the code chips can only be +1 or -1, the multiplication by these chips is achieved by changing the sign of the product as required.

3. A LOW POWER MC-CDMA ARCHITECTURE

The power consumption of a circuit can be cut by reducing the amount of switching. In the MAC based architecture, both inputs to the multiplier are switched every clock cycle as new input data samples and equaliser coefficients are multiplied. Since the multiplier is the largest component in the circuit, reducing the amount of switching here should have a large effect on the power consumption.

A block based approach [9] has previously provided an effective method for producing a low power DCT. In the case of a MC-CDMA receiver, a similar approach can be applied, if it is assumed that the channel fading is sufficiently slow that it allows the use of the same channel equalisation coefficient for a significant block length.

Under these conditions, a block of data containing M symbols can be buffered. The data is then processed, one carrier at a time for the entire block length of symbols. A block of memory is used to store the accumulated total for each symbol, and the MSB of each word provides the data estimate for each symbol. Figure 5 shows the architecture for this circuit.

The detailed operation of this architecture proceeds as follows. The first symbol of the first carrier is processed. This first symbol is a pilot and both the real and imaginary values are used to set the appropriate coefficient value. The sign of this coefficient is also dependent on the CDMA code chip for the first carrier. The remainder of the real parts of the symbols from the first carrier are then multiplied by the real part of the equaliser coefficient, and stored in separate addresses in the accumulator memory. The imaginary parts of the first carrier are then also processed, multiplying by the imaginary part of the equaliser and then being subtracted from the acummulator memory values to produce the desired real component of the complex multiplication. The algorithm then moves onto the second carrier. This is processed in the same way as the first except that the real products are added to accumulator memory. The remaining carriers are processed in the same way, a block at a time, until all the carriers have been processed. At this point, the most significant bit in each of the accumulator memory elements indicates each transmitted symbol value.

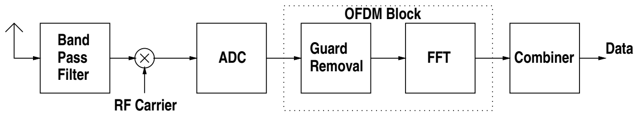

Figure 3: Multi-Carrier CDMA Transmitter

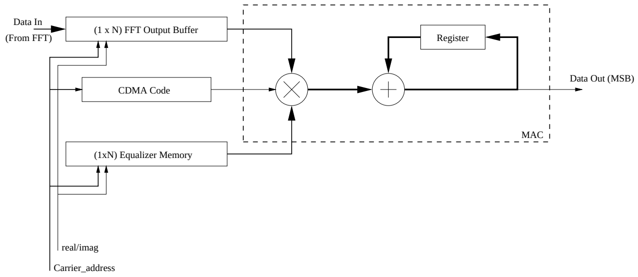

Figure 4: Combiner incorporating Multiply Accumulate Circuit

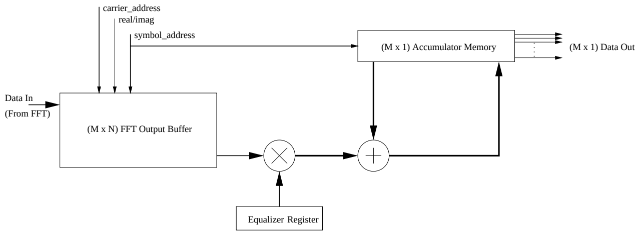

Figure 5: Low Power Block Based Combiner

The principal result of this architecture is that the equaliser coefficient and the CDMA code are held constant for M clock cycles, therefore one input to the multiplier is switched at a much lower frequency and hence the resulting power consumption should be significantly lower.

4. CIRCUIT SYNTHESIS

To evaluate the power consumption of the proposed architecture, both the MAC based combiner and the low power block based combiner were simulated in Verilog. A 64 carrier system was assumed and the data were divided into blocks of 32 symbols, with the first symbol in the block being used as a pilot for channel estimation. A word length of 16 bits was assumed for the output data from the FFT block. Additional circuitry was included to estimate the channel coefficients, including a division circuit, however the multiply unit can be reused. These do not increase the power consumption significantly as they are only used for 1 out of 32 symbols.

The circuits were simulated and verified using Verilog-XL. The circuits were then synthesised using Ambit Buildgates and the Alcatel 0.35μ library. This resulted in a MAC based circuit with cell size of 28166 gates and a block based circuit with cell size of 14415 gates.

Table 1 shows the area used by the main components in the MAC architecture. This is dominated by the equaliser memory,

Cell	Area
eq_mem	20521
mac1	3209
div1	3645
FSM	91
Total	28166

Table 1: Cell Area in MAC Architecture

Cell	Area
data_mem	6827
mul	2563
add1	457
div1	3636
FSM	172
Total	14415

Table 2: Cell Area in Block Architecture

which takes up more than two thirds of the total area. The division circuit and MAC unit also require sizeable areas, with the other sub-components requiring little circuit area.

Table 2 shows the area used by the block architecture circuit. In this case, the area required for accumulator (data) memory is significantly less than (just more than a third of) that required for the equaliser memory in the MAC architecture. The MAC circuitry is split into a separate multiply and add circuits, and there is a small reduction in area compared with the MAC due to the removal of the register. As would be expected the division circuit requires almost the same area. The control circuitry (FSM) is more complex since it has to include an additional symbol counter, but this is not a significant change in size compared to the other subcomponents.

5. POWER ANALYSIS

Power analysis was performed on the synthesised model using Synopsis Design Power assuming a clock rate of 10 MHz and data symbol rate of 156 kHz. This analysis was restricted to measuring the dynamic power consumption due to switching. Simulations were performed using a single user scenario and a scenario with an additional 15 interfering users modelling typical performance of the system.

Random CDMA codes were generated for the pilot symbols and for one user. The data for the single user scenario were generated by spreading known pilot symbols and random binary data symbols by CDMA codes. The spread symbols were multiplied by complex Gaussian random variables to model the effect of passing through parallel Rayleigh fading narrowband channels, and giving the appropriate value for the FFT output at the receiver. No explicit Gaussian additive noise was added, and the noise variance parameter in the MMSE equaliser, λ, was set arbitrarily to the value of 1. For the scenario with 15 interfering users, Gaussian distributed noise was added to the signal at the power level of 15 interfering users.

The switched power consumption for both circuits is shown in table 3. It is clear that the block architecture significantly reduces the power consumed in both cases to a level that is approximately half that of the MAC based architecture.

Architecture	Power (1 User)	Power (16 Users)
MAC	26.7923 mW	25.9522 mW
Block	12.9790 mW	13.9464 mW

Table 3: Comparison of MAC Based and Block Based Architectures

Cell	Power/mW
eq_mem	4.7162
mac1	3.8494
div1	0.2928
chip_mult	0.1085
Total	9.164

Table 4: Power Consumption in MAC Architecture Cells

A more detailed breakdown of the single user simulation power consumption of the MAC architecture circuit is shown in table 4. This shows the internal power consumption of the 4 highest power subcircuits along with the total internal power used in all cells. Clearly most of the power is used in the equaliser memory and the MAC unit. The divider circuit (used to calculate the MMSE coefficients) requires less than a 10th of the power of either circuit which is not surprising since it is only used when pilot symbols are received. The chip multiplication also consumes only an insignificant proportion of the power.

Table 5 shows a breakdown of the net switching power used in the MAC architecture circuit, detailing the 4 nets with highest switching power along with the total switching power within the main components and the total net switching power. Here the top two nets which are both in the equaliser memory consume more than a third of the total switched power. However the total power consumed by the memory block is only slight larger than the power consumed within the MAC unit, and these two circuits combined account for over 90% of the net switching power.

Table 6 shows a breakdown of the internal cell power used by the main components in the block based architecture circuit. The accumulator memory consumes the most power however this is less than half the consumption of the equaliser memory block in the MAC architecture circuit. The multiply and addition circuits require 1.11mW together, which is less than a third of the power required for the MAC unit. A slight reduction in power is also observed in the division circuit. Overall the internal cell power requirement is significantly less than half that of the MAC based architecture.

Most of the circuit power is however consumed switching nets. Table 7 shows the net switching power used by the block based architecture circuit in detail, again showing the power requirements of the 4 most active nets. Only one net contained within the accumulator memory requires a substantial quantity of power. This

Net	Power/mW
eq_mem/n_20563	3.1594
eq_mem/n_14368	3.1101
eq_mem/n_22357	0.9021
mac1/reg1/n_5275	0.1092
eq_mem	8.3895
mac1	7.6811
Total	17.6284

Table 5: Power Consumption in MAC Architecture Nets

Cell	Power/mW
data_mem	2.2285
mul	0.5902
add1	0.5244
div1	0.2068
chip_mult	0.0034
Total	3.683

Table 6: Power Consumption in Block Architecture Cells

net consumes most of the power used by the accumulator (data) memory block, and the total power consumption is half that of the equaliser memory block in the MAC circuit. The reduction of net switching power within the multiplication and addition circuits is more substantial, reducing the total power consumed here by a factor of 4. These circuits only account for two thirds of the total net switching power. The majority of the remainder is consumed switching the nets connecting the accumulated output of the add to the memory block (mem_write[x]) which consume a total of 2.25 mW. The total net switching power for the whole circuit is still however approximately half that of the MAC architecture circuit. And this produces the result that was shown in table 3, that the total power consumption is halved. This reduction occurs not only through the reduction in switching in the multiply circuitry, but also beacuse of a reduction in switching in the built in memory block, which is significantly smaller in block based circuit.

This reduction is however due to the block size and number of carriers: the 128x16 bit words of memory required for 64 complex equaliser coefficients are replaced by 32x32 bit words for accumulating the products. Therefore for different block sizes and numbers of carriers, the benefit may not be the same. This also does not take into account the larger buffer for storing FFT outputs which would be required and this would actually make the block based architecture significantly larger, however since this memory is accessed no faster than the smaller memory of MAC architecture, then the switched power consumption should not increase significantly.

6. CONCLUSIONS AND FUTURE WORK

This paper has presented detailed analysis of a low power multi-carrier CDMA receiver which can implement the MMSE multi-user detection algorithm. By processing the data in blocks, the rate of switching in the multiply circuit could be significantly reduced, and therefore a power reduction achieved. The low power architecture also reduced the size of the frequently accessed memory within the combiner circuit which resulted in further power reductions producing a final circuit which consumed only half the power of a more conventional MAC based architecture. Only the power consumption of the combiner block was considered here, however a full MC-CDMA receiver also requires a FFT block which will also have a significant power consumption. Therefore future work will consider the combination of the FFT and combiner circuits into a full receiver, possibly incorporating an extension of the block based approach to the FFT circuit.

Net	Power/mW
data_mem/n_9934	3.4980
mem_write[11]	0.1087
mem_write[10]	0.0959
mem_write[14]	0.0909
data_mem	3.9248
mul	1.1151
add	1.0307
Total	9.2959

Table 7: Power Consumption in Block Architecture Nets

7. ACKNOWLEDGEMENT

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