Power Driven Routing Using a Genetic Algorithm

B. M. Goni, T. Arslan
Department of Electronic and Electrical Engineering, University of Edinburgh,
The King's Buildings, Edinburgh, EH9 3JL, United Kingdom

And

B. Turton
Cardiff School of Engineering, Cardiff University,
Cardiff, CF2 3TF, United Kingdom

I. INTRODUCTION

Due to the increasing complexity of VLSI circuits and their frequent use in portable applications, energy losses in the interconnections of such circuits have become significant [1]. In the light of this, an efficient routing of these interconnections becomes important.

In the physical design process for very large scale integrated (VLSI) circuits the logical structure of a circuit is transformed into its physical layout. Detailed routing is one of the tasks in this process. A detailed router connects pins of signal nets in a rectangular region in accordance with a set of routing constraints, such as the number of layers, the minimal space between wires, minimum wire width, number of vias, crosstalk and the net length. The results of this detailed routing has a strong influence on the fabrication yield and production costs of the circuit [1].

Traditional channel routing algorithms have proved very successfull in reducing channel height [2, 3]. Any further reductions are only possible if some nets are routed "outside" the channel [4]. Based on this observation, some researchers have proposed utilisation of over-the-cell area to obtain further reduction in the channel height [4-8]. This style of routing is called over-the-cell channel routing. As more metal layers are becoming available for routing in the standard cell design style, routing over the cells becomes both practical and important.

The inclusion of both over-the-cell and channel optimisation in a single channel routing domain will provide an effective framework for area/energy optimisation. However, this will increase the burden on the routing algorithm due to the significant increase in search space. To cope with this multi-objective search problem, evolutionary algorithms, such as Genetic Algorithms (GAs) have been employed [9-16].

In this paper, we study the effect of an evolutionary over-the-cell router, developed by the authors, on energy loss and area reduction in all channel areas and compare this with a traditional over-the-cell router [8]. We show that significant reductions in energy loss are achieved by the evolutionary over-the-cell router in all the channel areas. Up to 46% reductions in area and energy loss is achieved in the channel area. In addition our algorithm achieves up to 71% and 61% reductions in area and energy loss in the top and bottom over-the-cell areas. Our algorithm achieves up to 56% energy loss and area reductions for all the channel areas top, bottom and internal put together, when compared with the best of the traditional over-the-cell routers.

The following expression establishes the relationship between energy loss and area:

$$W = \frac{1}{2}\frac{\varepsilon A}{d}V^2 \qquad (1)$$

Where ε is the dielectric constant, A the area, d thickness of the insulator and V is the voltage.

In a routing problem the main objective is to reduce area, which is done by minimising the track requirement in the channel and over-the-cell areas [1, 4]. This direct effect on channel height (and hence area), implies that the number of tracks T is proportional to area A ($T \alpha A$). From equation (1) this implies that reducing the number tracks by a certain factor, also reduces area and consequently energy loss by the same amount.

II. THE EVOLUTIONARY ALGORITHM

General properties: A traditional GA-based algorithm was used for this work. The developed algorithm is based on a model developed by Goldberg [17]. Our investigations revealed that with a population of 500 chromosomes, the following GA characteristics are necessary for a performance which provides a 'good' trade off in speed and quality of solutions:

- Two point crossover and random mutation at rates of 0.6 and 0.001.
- Chromosome selection procedure using Baker's Stochastic Universal Sampling algorithm [18, 19].
- Employment of an elitist selection strategy [19].

The chromosome structure for a single net X is presented as [top,int,bot,id]. Where, top = top track on which net X is placed; int = internal track on which net X is placed; bot = bottom track on which net X is placed; id = the net number.

Fitness function: A key component of the GA is the fitness evaluation stage, where the quality of the different routing solutions are assessed. Beginning with a given netlist (see Figure 1), and after initialisation, the fitness function starts by identifying all multi-terminal net circuit segments for over-the-cell routing, and places them on tracks over-the-cell according to horizontal constraints. Further, it proceeds to route the remaining net circuits inside the channel subject to horizontal and vertical constraints. For a given structure Y, the fitness function F(Y) can be specified as:

F(Y) = OTC(Y) + HV(Y) + VV(Y).

Where OTC, HV and VV are routing procedures and are described as follows:

Over-the-cell routing (OTC): Performs the routing of multi-terminal net circuits in the over-the-cell areas, and returns their number. After this procedure only net circuits with single pin connections at both the top and bottom will remain inside the channel area.

Horizontal violation elimination (HV): Carries out the elimination of horizontal violations [20], by returning the number of net circuits without such violations. It is applied to both the over-the-cell and channel areas.

Vertical violation elimination (VV): Performs the elimination of vertical violations [20], by returning the number of two pin (terminal) net circuits connected to the top and bottom pins inside the channel area without such violations. As there are no vertical violations in the regions over-the-cell, this procedure is not applied.

Two or more net circuits are placed on the same track if they are without horizontal and vertical violations in the channel area. For the over-the-cell areas only the elimination of horizontal violations need to be satisfied before net circuits are routed on the same track. This is illustrated using the Yoshimura-Kuh channel circuit in [2], the algorithm starts by first identifying top and bottom multi-terminal net circuits and routes them over-the-cell (nets 1,2,3,4,5,8,9 and 10) as shown in Figure 2. It then carries out routing for those net circuit segments that must remain fully or partially within the channel area, (nets 5,6,7 and 9). In the process it identifies those nets that can be placed on the same track (nets 5,6, and 9) resulting in track savings. It is evident that our algorithm requires only two rows (tracks) to route this channel circuit, compared to five in [2]. The four net circuits left in the channel are all two terminal nets. Vertical and horizontal segments of nets are placed on the first and second layers respectively in the channel area (VH model).

III. RESULTS

Table 1 compares our algorithm with recent work using similar implementation strategy (e.g CMOS process technology) [8] for all the areas i.e Top, Bottom and Internal. Overall our algorithm provides better performance. For example, with 3c our algorithm obtains solutions of 12 and 9 tracks for the top and bottom over-the-cell areas respectively, compared to 15 and 16 tracks achieved for the same areas in [8]. Inside the channel our algorithm obtains a solution using 11 tracks compared with 15. This amounts to reductions in area and consequently energy loss of 20%, 43% and 26% in the top, bottom and channel areas respectively. The greatest reductions in energy losses are 71%, 61% and 46% in the top (EX4b), bottom (EX5) and channel (EX3a) areas respectively. For complete comparison of our algorithm and that in [8], Table 2 shows the total percentage reductions in area and energy loss for the entire channel region (Top, bottom and internal). For example, with benchmark example 1 our algorithm achieves up to 33% reductions in energy loss and area for all areas put together. Also with example 4b, our algorithm achieves up to 56% reductions in power loss and area.

IV. CONCLUSIONS

A concurrent evolutionary over-the-cell router is presented and its effects on energy loss and area reduction has been studied. Results obtained are compared with those of a traditional over-the-cell router. Significant reductions in energy loss is achieved by the evolutionary over-the-cell router in all channel areas. Reductions of up to 46% in area and energy loss is achieved in the channel area. In addition the algorithm achieves up to 71% and 61% reductions in area and energy loss in the top and bottom over-the-cell regions. Overall, our algorithm achieves up to 56% energy loss and area reductions for all the channel regions top, bottom and internal put together, when compared with competing algorithms in the literature.

REFERENCES

[1] N. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer Academic Publishers, 1995.

[2] T. Yoshimura, and E. S. Kuh, “Efficient algorithms for channel routing,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* CAD-1(1):25-35, January, 1982.

[3] R. Joobbani, “An artificial intelligence approach to VLSI routing,” Boston, MA, Kluwer, 1986.

[4] L. Chang, P. Hsiao, J. Yan, and P. Shew, “A robust over-the-cell channel router,” *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 12, no. 10, pp 1592-1599, october 1993.

[5] N. Holmes, N. Sherwani, M. Sarrafzadeh, “ Utilisation of vacant terminals for improved over-the-cell channel routing,” *IEEE Transactions on CAD of Integrated Circuits and Systems,* 1993.

[6] M. S. Lin, H. W. Perng, C. Y. Hwang, and Y. L. Lin, “Channel density reduction by routing density reduction by routing over the cells,” *Proc. 28th Design Automation Conf.*, pp. 120-125, 1991.

[7] J. Cong, and L. Liu, “Over-the-cell channel routing ,” *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 9, pp 408-418, April 1990.

[8] Y. Shiraishi and Y. Sakemi, “A permeation router,” *IEEE Transactions Computer-Aided Design*, Vol. CAD-6, pp. 462-471, May 1987.

[9] B. B. Prahlada Rao, L. M. Patnaik and R. C. Hansdah, “A Genetic algorithm for channel routing using inter-cluster mutation,” *IEEE*, pp 97-103, 1994.

[10] J. Lienig, and K. Thulasiraman, “A new genetic algorithm for the channel routing problem,” *7th International Conference on VLSI Design*, pp. 133-136, January 1994.

[11] J. Lienig and K. Thulasiraman, “A genetic algorithm for the channel routing of VLSI circuits,” *Evolutionary Computation*, vol. 1, No. 4, pp. 293-311, 1994.

[12] N. Gockel, G. Pudelko, R. Dreschsler, and B. Becker, “A hybrid genetic algorithm for the routing of VLSI circuits,” *Proc. IEEE Int. Symp. Circuits and Systems*, 1996, pp 675-678.

[13] J. Lienig, “A parallel genetic algorithm for performance-driven VLSI routing,” *IEEE Transactions on Evolutionary Computation*, Vol. 1, No. 1, April 1997

[14] N. D. Davidenko, V. M. Kureichik, and V. V. Miagkikh, “ Genetic algorithm for restrictive channel routing problem,” *Proceedings of the Seventh International Conference on Genetic Algorithms*, pp. 636-641, 1997.

[15] T. Arslan, E. Ozdemir, M. S. Bright, and D. H. Horrocks, ”Genetic synthesis techniques for low-power digital signal processing”, *Proceedings of The IEE Colloquium on Digital Synthesis*, London, UK, pp. 7/1-7/5, 1996.

[16] M. S Bright, and T. Arslan, ”A genetic framework for the high-level optimisation of low power VLSI DSP systems”, *IEE Electronics letters*, Vol. 32, No.13, pp. 1150-1151, 1996.

[17] D. E. Goldberg, *Genetic Algorithms in search, Optimisation & Machine Learning. Addison-Wesley.* 1989.

[18] J. E. Baker, "Reducing bias and inefficiency in the selection algorithm." *Proceedings of the third International Conference on Genetic Algorithms.* Morgan Kaufmann Publishers. 1989.

[19] L. Davies, *Handbook of genetic algorithms*. Van Nostrand Reinhold. 1991.

[20] A. T. Rahmani, and N. Ono, “A genetic algorithm for channel routing problem,” *Proceedings of the 5th International Conference on Genetic Algorithms*, pp. 494-498, 1993.

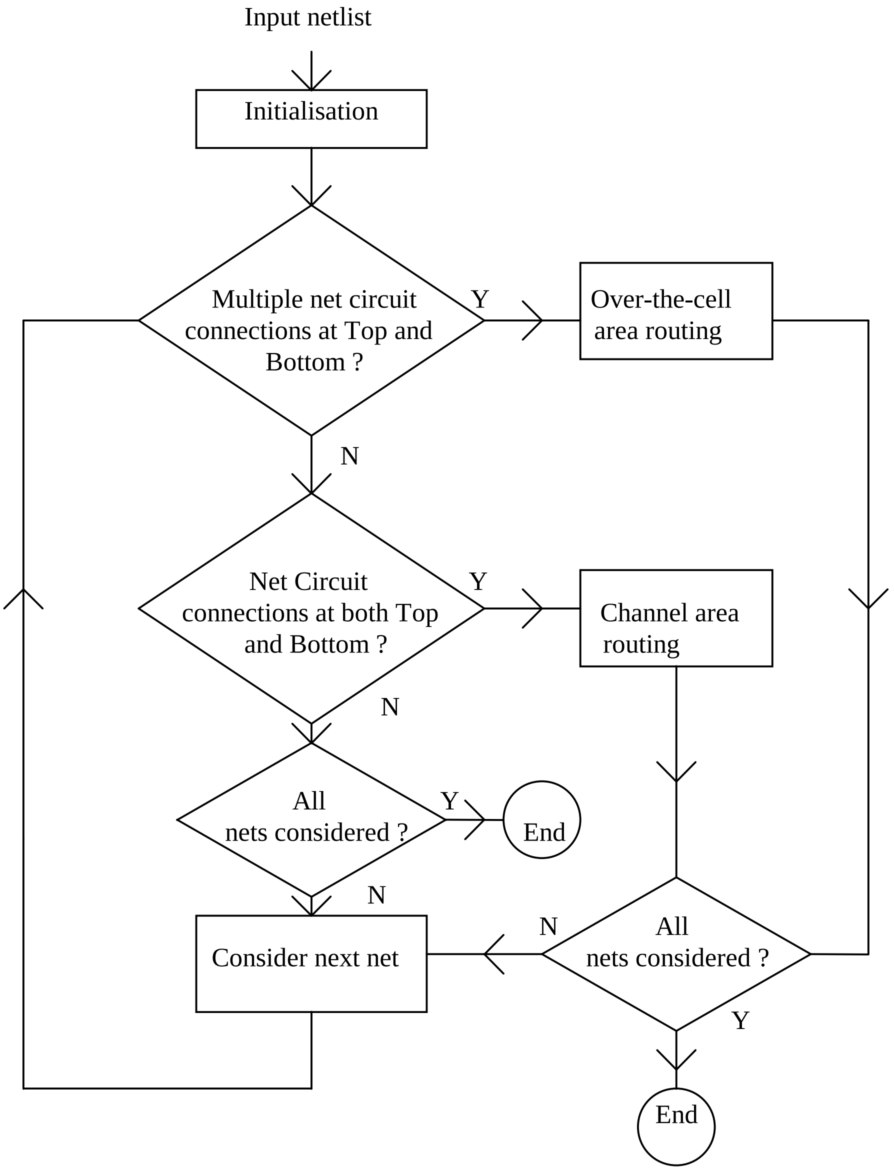

Figure 1: Fitness function flowchart

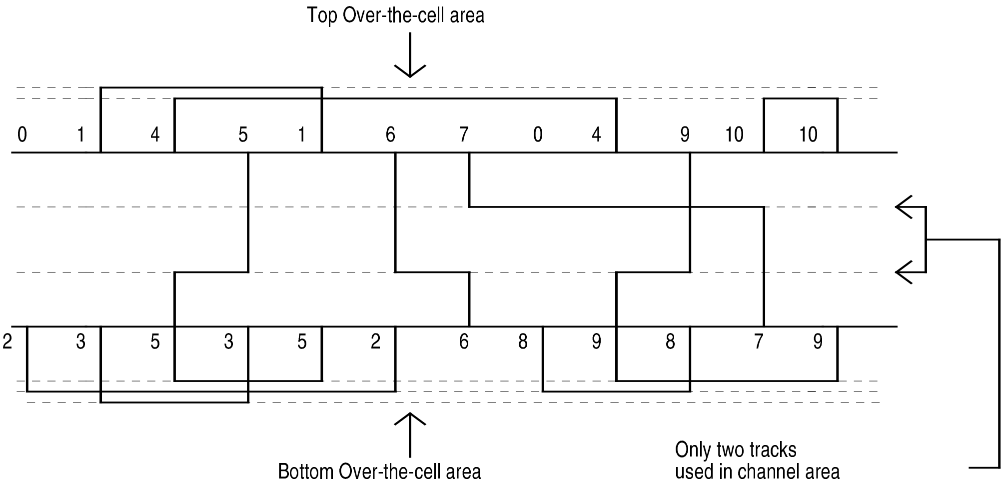

Figure 2: A realisation of the netlist in [2]

		[8]			Our Algorithm		
Example	Density	Top	Internal	Bottom	Top	Internal	Bottom
1	12	11	6	7	4	6	6
3a	15	13	15	10	9	8	6
3c	18	15	15	16	12	11	9
4b	17	28	6	24	8	6	11
5	20	24	9	18	10	9	7
De	19	20	13	19	14	13	14

Table 1: Comparison of our algorithm with the algorithm in [8] for all areas.

Example	[8] (track total)	Our Algorithm (track total)	Energy loss and area reduction
1	24	16	33%
3a	38	23	39%
3c	46	32	30%
4b	58	25	56%
5	51	26	49%
De	52	41	21%

Table 2: Comparison of our algorithm with the algorithm in [8] for all areas for energy loss and area reduction.