

# Reconfigurability-Power Trade-Offs in Turbo Decoder Design and Implementation

Indrajit Atluri<sup>1</sup> and Tughrul Arslan<sup>1,2</sup>

<sup>1</sup>*School of Engineering and Electronics, The University of Edinburgh, EH9 3JL, UK*

<sup>2</sup>*Institute for System Level Integration, Alba Centre, Livingston, EH54 7EG, UK*  
{ai, arslan}@ee.ed.ac.uk

## Abstract

*Reconfiguration between decoding algorithms, employed in the 3<sup>rd</sup> generation mobile communication standards such as the UMTS, cdma2000 is an added advantage, which facilitates the selection of the appropriate algorithm in any circumstance. The Log-MAP and the SOVA algorithms are the two main algorithms employed in the turbo codes, which are featured in the 3G mobile radio standards. In this paper, the authors examine the reconfiguration between a low power Log-MAP decoder and a SOVA decoder, and elaborate the advantages over a conventional Log-MAP decoder, in terms of low power/area consumption and the flexibility offered to a turbo decoder.*

## 1. Introduction

Reconfiguration has become an important issue, in today's diverging trend of the 3G Communication standards, apparent from the development of the UMTS in Europe and the emergence of cdma2000 in USA. Table (2) shows some of the main blocks and the techniques employed in the three major standards and services [5] – UMTS, cdma2000 and W-CDMA. Different service channels existing in each of the 3<sup>rd</sup> generation communication standards use different encoder types, each one of these have specified constraints on BER (Bit Error Rate) and delay and can have different input data rates. Thus, to facilitate greater flexibility in choosing the optimum algorithm, reconfiguration should be at the level of hardware. Turbo codes [1] have found a very wide range of applications mainly in wireless communications, ranging from the third generation mobile systems to deep-space exploration due to their capability of achieving a small BER (Bit Error Rate) of 0.7 dB, i.e., near-capacity performance in an additive white Gaussian noise (AWGN) channel. Since turbo codes employ either the SOVA [6] (Soft Output Viterbi Algorithm) decoder or the Log-MAP [2] (Maximum A Posteriori) decoder for the iterative decoding, the authors examine the various advantages of using a low power Log-MAP decoder in place of the

conventional Log-MAP decoder by analyzing the architectures of these decoders in detail.

## 2. Reconfigurability Features in Decoders

The reconfigurability features of the SOVA and the conventional Log-MAP decoder have been examined in [3]. If BER is the considered as the reconfiguration criterion, then at low BER, SOVA is preferred, even though both the SOVA and Log-MAP perform identically, since SOVA is less complex. But at high BER, Log-MAP is used as it gives better performance. If processing complexity is the reconfiguration criterion, then for low input data rates Log-MAP can be used and vice versa, in order to achieve the delay specification of the appropriate service channels. In the next few sections, these features and the advantages in using the low power Log-MAP decoder [4] for reconfiguration with SOVA decoder in a turbo decoder, instead of the conventional Log-MAP decoder are examined. The main blocks in all the three decoders are as follows:

### 2.1. Branch Metric Calculator Block (BMC)

The branch metric calculator block is common in all the three decoders – SOVA, Log-MAP and the modified Log-MAP algorithms. The corrupted information from the channel is taken in its quantized form as the input to the BMC. The BMC requires addition operations for evaluating the BMCs, hence the adders blocks are reconfigurable in all the decoders.

### 2.2. State Metric Calculator Blocks (SMC)

The forward state metric calculator (FSMC) and the reverse state metric calculator (RSMC) blocks in both the Log-MAP and the reduced complexity Log-MAP decoders have almost the same architecture and carry out the same number of operations. The only difference is the initialization of the state metric values. In a SOVA decoder only the forward state metrics are required. In both the Log-MAP decoders, the state metric calculator

consists of the following sub-blocks which are detailed below:

**2.2.1. Path Metric Calculator (PMC).** The path metric calculator blocks evaluate the path metrics by adding the branch metrics and the state metrics at that time instant in the trellis structure. This addition operation is reconfigurable in this block in all the three decoders.

**2.2.2. Survivor Path Calculator (SPC).** In this block the path metrics are compared and the absolute difference is evaluated. Also, the maximum value of the two competing path metrics is selected in the case of a SOVA, and the minimum value in the case of the Log-MAP decoders. This minimum path metric value along with the absolute difference is used to evaluate the 'E' function value in the FEC block, which is defined as  $a \oplus b = -\ln(e^{-a} + e^{-b})$  which is rewritten as  $\min(a,b) - \ln(1 + e^{-|a-b|})$ . In the low power Log-MAP decoder the 'E' function is defined in a different way as  $a \oplus b = -\ln(e^{-a} - e^{-b})$  which is rewritten as  $\min(a,b) - \ln(1 - e^{-|a-b|})$ . The compare and select operation in the ACS (Add-Compare-Select) are common in all the three decoders. In addition to the compare, select operations the Log-MAP decoders require an additional FEC block.

**2.2.3. Forward Eccumulator Calculator (FEC).** The absolute difference from the SPC is used to output the value of the log function  $[-\ln(1 - e^{-|a-b|})]$  from the look-up table (LUT) in the low power Log-MAP decoder. The LUT is used in the FSMC, RSMC and the LLRC blocks in both the Log-MAP decoders. The FEC block is a common block in both the Log-MAP decoders and is not required in the SOVA decoder. The low power Log-MAP decoder consists of an additional block – the FRSMC (Forward recursive reverse state metric calculator) block which evaluates the reverse state metrics in the forward recursive manner. This block is an addition to the hardware and is absent in SOVA and the conventional Log-MAP decoders. But the FRSMC block comprises of the same sub-blocks as in the SMC blocks – the PMC and the SMC, which perform similar operations, except the FEC block in which the eccumulator function is different from the one in the conventional decoder. Hence, addition is the only reconfigurable operation in this FEC block.

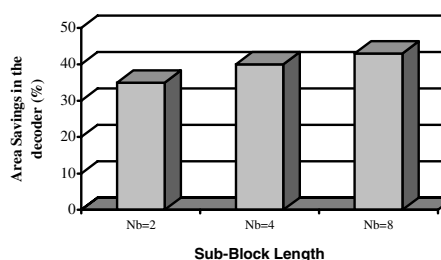
### 2.3. Log likelihood Ratio Calculator (LLRC)

The log-likelihood ratio calculator in the low power Log-MAP decoder requires the same add-compare-select operations, along with the LUT to evaluate the final decoded outputs. Thus, the LLRC block is similar to the one in the conventional Log-MAP decoder.

## 3. Advantages and Results

The advantage of using the low power Log-MAP decoder instead of the conventional Log-MAP decoder for reconfiguration with the SOVA decoder in a turbo decoder is offering extra flexibility for the turbo decoder to adapt for the channel requirements and accordingly employ the appropriate component decoder. The common reconfigurable features between SOVA, Log-MAP and the reduced complexity Log-MAP decoders discussed explicitly in Section (2) are summarized in Table (1).

The Log-MAP decoders have been designed at register transfer level (RTL) using Verilog HDL. The cores were synthesized using Synopsys *DesignCompiler* with UMC 0.18 $\mu$  standard cell CMOS library and the power consumptions were estimated using the Synopsys *DesignPower* tool. The modified Log-MAP decoder offers low power consumption. It consumes up to 35% (for sub-block length  $N_b=8$ ) less power than the conventional Log-MAP decoder. Apart from this the authors have observed a range of savings in area consumption (Figure (1)) in the low power Log-MAP decoder for different sub-block lengths (for  $N_b=2, 4$  and 8). This decoder reduces storage requirements and the entire frame is processed at a time unlike the sliding window Log-MAP decoder [7] which does not make use of the information in the whole frame.



**Figure 1: Area savings for various sub-block lengths over conventional decoder.**

## 4. Conclusions

In the reconfiguration of the SOVA and Log-MAP decoders in a turbo decoder, it can be concluded that employing our low power Log-MAP decoder in place of the conventional Log-MAP decoder reduces overall power and area consumption in a turbo decoder apart from retaining all the common reconfigurable operations, and maintaining flexibility to choose the optimum decoder.

## 5. References

- [1] C.Berrou, A.Glavieux, and P.Thitimajshima. Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-Codes. Proc. ICC '93, Pages 1064-1070, Switzerland, May 1993.
- [2] P. Robertson, E. Villerbrun, and P. Höher, "A Comparison of Optimal and Sub-Optimal MAP Decoding Algorithms Operating in the Log Domain," Proc. of the International Conference on Communications, pp. 1009-1013, June 1995.
- [3] C.Chaikalis, M.Salimi-Khaligh, N.Panayotopoulos and J.M.Noras, "Reconfiguration between soft output Viterbi and Log Maximum A Posteriori Decoding Algorithms," IEEE 3G Mobile Comm. Technologies Conference. 2000, pp. 316-320.
- [4] I.Atluri and T.Arslan, "Low Power VLSI Implementation of the MAP decoder for Turbo Codes through forward recursive calculation of Reverse State Metrics," IEEE International SoC Conference 2003, pp. 408-411.
- [5] Riera-Palou, C.Chaikalis and James M.Noras, "Reconfigurable Mobile Terminal Requirements for Third Generation Applications", IEE Colloquium on UMTS Terminals and Software Radio 1999, pp. 9/1-9/6.
- [6] J.Hagenauer and P.Hoehner, "A Viterbi algorithm with soft-decision outputs and its applications," Proc. Globecom, Nov. 1989, pp. 1680-1686.
- [7] S.Benedetto, D.Divsalar, G.Montorsi, and F.Pollara, "Soft-output decoding algorithms in iterative decoding of turbo codes," JPL TDA Progress Report, vol. 42-124, Feb 15, 1996.

**Table 1: Common reconfigurable operations between SOVA, Log-MAP and low power Log-MAP decoders.**

	BMC	FSMC			RSMC			LLRC	FRSMC			PUU
		FPMC	SPC	FEC	RPMC	SPC	FEC		PMC	SPC	FEC	
<i>SOVA</i>	Add	Add	Compare & Select									Compare & Select
<i>Log-MAP</i>	Add	Add	Compare & Select	Add & LUT	Add	Compare & Select	Add & LUT	ACS & LUT				
<i>Low Power Log-MAP</i>	Add	Add	Compare & Select	Add & LUT	Add	Compare & Select	Add & LUT	ACS & LUT	Add	Compare & Select	Add	

**Table 2: Standards and the respective techniques employed.**

STANDARD	CHANNEL CODING	MODULATION	MULTIPLE ACCESS
<i>UMTS (Europe)</i>	RS+Convolutional: Rate= 1/2, 1/3, L=9 (OR) Turbo: Rate= 1/2, 1/3	Not Known at Present	TDMA/W-CDMA
<i>CDMA2000 (USA)</i>	CRC+Convolutional: Rate= 1/2, 1/3, 1/4, L=9 (OR) CRC+Turbo: Rate= 1/2, 1/3, 1/4, L=4	BPSK/QPSK	FDMA/CDMA2000
<i>W-CDMA (Japan)</i>	CRC+Convolutional: Rate= 1/3, L=9 (OR) CRC+Turbo: Rate= 1/3, L=3	BPSK/QPSK	TDMA/W-CDMA