

# A Delay Spread Based Low Power Reconfigurable FFT Processor Architecture for Wireless Receivers

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## Abstract

*This paper proposes a novel concept of adjusting the FFT size in real time as per the delay spread in wireless receivers. The FFT size in OFDM/MC-CDMA based wireless receivers varies from 1024(1k)-point to 16-point. A low power reconfigurable radix-4 1k-point FFT processor architecture is proposed that can also be configured as a 256-point, 64-point or 16-point as per the channel parameters. By tailoring the clock of the higher FFT stages for longer FFT's, significant power saving is achieved by switching to shorter FFTs from longer FFTs.*

## 1. Introduction

The critical design issue for future wireless receivers is the combined requirements for high-performance, low power and flexibility. The wireless systems have diverse application requirements in the form of changing data rate and bit error rate along with changing bandwidth and other channel parameters like the delay spread. It is desirable for wireless receivers to adapt their operation instead of being designed for the worst case scenario.

In multi-carrier systems like multi-carrier code division multiple access (MC-CDMA) or Orthogonal frequency division multiplexing (OFDM), the two most power consuming blocks in the receiver are the FFT and the Viterbi decoder [1]. Researchers have already investigated low power architectures for these two important blocks [2][3]. The way forward to reduce the power consumption further is to dynamically reduce the complexity of the receiver architecture in real time as per the changing channel requirements like the delay spread, signal to noise ratio (SNR), bandwidth and bit error rate etc. In [4], the researchers have shown the potential of saving power in a Viterbi decoder by dynamically varying its architecture according to real-time changes in system characteristics.

This paper proposes to adjust the FFT size in real time as per the channel delay spread instead of using a fixed large FFT based receiver designed for the worst case delay spread. The FFT size in MC-CDMA varies from 16-point FFT to 1k-point FFT [5] depending upon the delay spread, transmission rate and Doppler frequency.

Significant power saving is achieved by using the most appropriate FFT size instead of a fixed large size FFT for worst case channel conditions. This is achieved by monitoring the channel parameters like the delay spread, Doppler frequency and Transmission rate in real time. Reconfigurable radix-4 FFT processor architecture has been proposed that can also be configured as a 256-point, 64-point and a 16-point by tailoring the clocks of the higher stages in real time. The power saving in going down from 1024-point to 256-point is 63% and to 64-point is 83% and to 16-point is 92%. The hardware overhead in the form of logic for monitoring the delay spread is minimal because this logic has to operate at a much lower frequency.

## 2. MC-CDMA

MC-CDMA [5] is a spread spectrum technology which combines the advantages of OFDM and CDMA to produce a spectrally efficient multi-user access system. This wireless access system may be utilised in future mobile wireless systems and hence power consumption is an important issue.

In MC-CDMA, the coded user signal is transmitted on multiple sub-carriers. The resulting signal has a coded structure in the frequency domain. If the processing gain is equal to the number of sub-carriers then this system modulates all the sub-carriers with the same coded bit, but with a phase shift on each sub-carrier determined by the spreading code. This multi-carrier modulation can also be implemented using an inverse FFT. If the  $k^{\text{th}}$  chip of the spreading code for user  $u$  is defined as  $c(k,u) \in \{-1,+1\}$  then the transmitted baseband signal for the  $m^{\text{th}}$  coded data symbol  $b(m)$  is:

$$x(n) = \sum_{k=0}^{N-1} \exp(j2\pi kn / N) c(k,u) b(m) \quad (1)$$

The baseband signal is then cyclically extended by more than the channel delay spread to remove Inter-symbol interference (ISI). The block diagram of a MC-CDMA transmitter is shown in Figure 1.

By using a guard interval, the receiver selects the portion of the signal that is free from ISI. This is then processed by the FFT to demodulate the sub-carriers. The

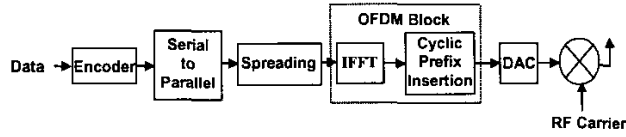


Figure 1. Multi-carrier CDMA transmitter

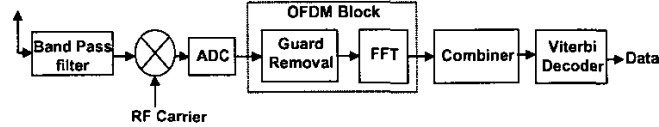


Figure 2. Multi-carrier CDMA receiver

channel effect of a multipath channel  $h(n)$  at the output of the FFT is narrowband for each sub-carrier,  $H(k)$ , and therefore equalisation and de-spreading can be incorporated into a single combining operation to estimate the soft bits for the decoder. The soft bits  $s(n)$  are fed to the Viterbi decoder to recover the transmitted bits. If the output of the FFT block at frequency bin  $k$  is defined as  $Y(k)$  then the combining operation can be represented by,

$$s(n) = \sum_{k=0}^{N-1} R\{c(k,u)A(k)Y(k)\} \quad (2)$$

The equaliser coefficients  $A(k)$  are obtained by inserting pilot bits in the transmitted bit stream. A MC-CDMA receiver contains three main system blocks, an FFT block to demodulate the OFDM signals, a combiner block and a Viterbi decoder for decoding the Convolutional codes. The simplified receiver block diagram is shown in Figure 2.

### 3. Dependence of FFT size on channel parameters

In basic OFDM system, a guard interval popularly known as cyclic prefix is inserted in every symbol to overcome the effect of ISI. The guard interval needs to be longer than the delay spread of the channel. The OFDM symbol duration is chosen to be about 5 times longer than the guard interval in the interests of transmission efficiency [1]. The number of sub-carriers (FFT size) is determined by the following,

$$(\text{OFDM symbol duration-guard interval}) * \text{bandwidth.}$$

In MC-CDMA, the number of sub-carriers depends upon the delay spread ( $\tau$ ), maximum Doppler frequency ( $f_d$ ) and the transmission rate ( $R$ )[5]. Figure 3 shows the variation of the optimum number of sub-carriers as a function of the normalised value of delay spread ( $\tau * (R * P)$ ), where  $P$  is the processing gain for different values of the normalised maximum Doppler frequency  $Nfd$  ( $f_d / (R * P)$ ) [5]. It is clear from Figure 3, that for the

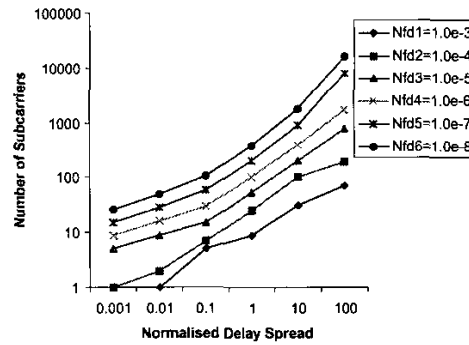


Figure 3 Optimum number of sub-carriers as a function of normalised delay spread and maximum Doppler frequency.

intermediate range of  $\tau$ ,  $f_d$  and  $R$ , the optimum number of sub-carriers vary from 16 to 1024. Only in extreme cases the optimum number of sub-carriers go beyond this range. The bottom plot corresponds to  $Nfd1 = 10^{-3}$ , whereas the top plot corresponds to  $Nfd6 = 10^{-8}$ .

It has been clearly established that in both MC-CDMA and basic OFDM, the number of sub-carriers (FFT size) is a strong function of the delay spread. Since the indoor delay spread is measured in the range from 30ns to 370ns depending on the building size [1] and the outdoor delay spread is much longer, it is desirable to design a reconfigurable FFT processor whose size can be tailored as per the channel parameters like the delay spread maximum Doppler frequency and transmission rate in real time. The basic idea is to design the receiver for the maximum number of sub-carriers (FFT size) and then clock gate unused blocks for the smaller sizes depending upon the delay spread. The combiner architecture can also be made reconfigurable by clock downing the unused segmented memory used for storing the equaliser coefficients for smaller number of sub-carriers. This approach of hardware size adjustment on the basis of changes in the channel parameters in real time can be extended to other blocks of the receiver like the Viterbi

decoder for saving even more power.

The switching to the appropriate FFT size, combiner, and Viterbi decoder architectures will be done automatically by the receiver after reading channel parameters like the delay spread, SNR and bit error rate in real time. This reading operation has to be carried out at a much lower frequency than other operations and hence the power overhead is minimal.

The reconfigurable FFT processor is based on Bi & Jones radix-4 pipelined architecture [6]. It is better than other pipelined architectures in terms of computational efficiency and hardware savings in complex multipliers, adders and data stores. It consumes less power due to less hardware requirement as compared to the other radix-4 pipelined architectures.

### 5. Reconfigurable FFT architecture

A reconfigurable radix-4 1024-point pipelined FFT processor architecture comprises of five radix-4 stages as shown in Figure 4. Reconfigurability is achieved by inserting three multiplexers namely MUX I, MUX II and MUX III between the higher stages for directly routing the input data to stage 2, stage 3 or stage 4 depending upon the required FFT size. The FFT processor can act as a 256-point processor by feeding the input data directly into stage 2 and clocking down the first stage. This is accomplished by selecting the input data rather than the output of stage 1 by the external select input  $S_{256}$  of MUX I. Moreover, the gated clock input (G\_ck1) to stage 1 is also disabled by the FFT Finite state machine (FFSM). Similarly, it can act as a 64-point processor by controlling the select input  $S_{64}$  of MUX II to feed the input data directly into stage 3 and disabling stage 1 and stage 2 with the help of gated clocks G\_ck1 and G\_ck2. In the end, it can also act as a 16-point processor by feeding the input data directly into stage 4 with the help of select line  $S_{16}$  of MUX III and disabling clocks for stage 1, stage 2 and stage 3 using G\_ck1, G\_ck2 and G\_ck3.

The basic stage of the FFT processor comprises of a commutator, a butterfly and a complex multiplier as shown in Figure 5. The last stage contains just the

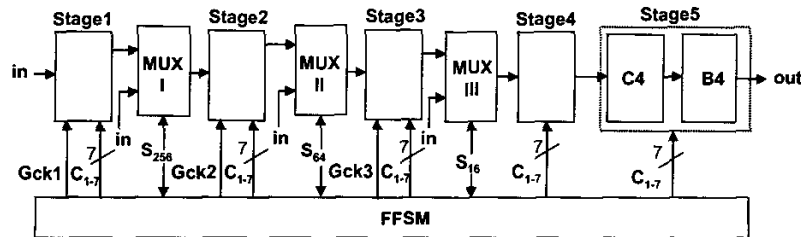


Figure 4. Architecture of 1024-point radix-4 reconfigurable pipelined FFT processor

commutator (C5) and the butterfly (B5).

The commutator, shown in Figure 6 [6], is based on six  $N_t$  length FIFO's along with three multiplexers. The FIFO block within the commutator structure is realised using dual port RAM for saving power consumption. The FIFO size  $N_t$  equals  $4^{(t-1)}$ , where 't' is the stage number.

The FFT Finite state machine (FFSM) is responsible for generating all the control signals for all the FFT stages. It is a combination of four different finite state machines (FSM) i.e. one FSM per stage. Each FSM generates seven control signals  $C_{1-7}$  for its stage. The MUX I, MUX II and MUX III select lines are activated by the external inputs as per the FFT size.

### 6. Simulation results

The reconfigurable FFT processor core has been designed at the register transfer level (RTL) using Verilog hardware description language. The core was synthesized using SYNOPSIS *DesignCompiler* with UMC 0.18 $\mu$  standard cell CMOS library. It was then followed by gate level netlist simulations with SYNOPSIS Standard delay format (SDF) for 4000 uniformly distributed random input data samples for all the FFT lengths using Verilog-XL<sup>TM</sup> simulator. The resulting switching activity of the circuit nets was then used by the SYNOPSIS *DesignPower* to compute the power consumption for the different FFT sizes. All the simulations were carried out at a clock frequency of 20MHz. The results are listed in Tables 1 and 2. Table 1 lists the power saving for short FFT's as compared to 1024-point FFT. There is considerable power saving in going down from 1024 point FFT size to 16-point FFT size. The power saving is 92% for a 16-point FFT, 83% for a 64-point FFT and 63% for a 256-point

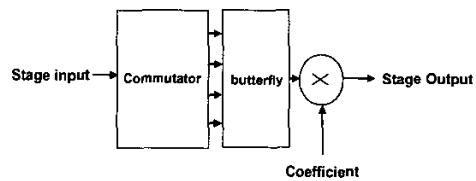


Figure 5. General stage of a radix-4 FFT processor.

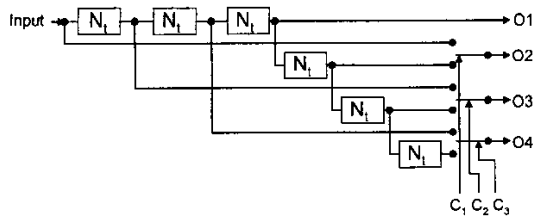


Figure 6. Radix-4 Commutator Architecture

Table 1. Power consumption comparison

FFT size	Power consumption in mW	% Power reduction
16	24.71	92
64	51.29	83
256	109.92	63
1024	296.60	-

Table 2. Power consumed by the different stages of the 1k-point FFT Processor

Stages of FFT processor	Power consumption in mW	% Power contribution
Stage 1	186.65	63
Stage 2	58.63	20
Stage 3	26.58	9
Stages 4 and 5	24.71	8

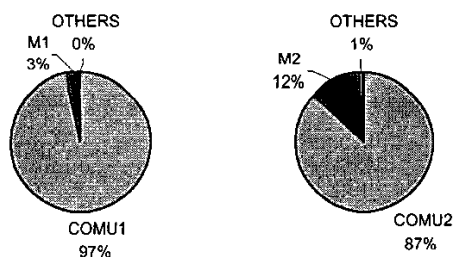


Figure 7. Percentage Power consumption of stage1 and stage2 blocks of the FFT processor.

point FFT. It is evident from Table 2 that stage 1 contributes 63% power consumption followed by stage2, stage 3 and then the last stages. It is also clear from Figure 7 that stage 1 commutator (COMU1) consumes 97% of stage 1 power consumption followed by multiplier (M1). This is due to the large size of dual port RAM required to implement long FIFOs. The remaining blocks (OTHERS) of stage 1 consumes very little power consumption. In stage 2, the power share of the commutator (COMU2) reduces to 87%. This downward trend of commutator power consumption continues for stage 3 to stage 5 as well due to the reduction in FIFO sizes required from

stage1 to stage 5.

The reconfigurable architecture overhead is minimal in the form of multiplexers and some logic for clock gating. The clock gating signal will remain active for a much longer duration as compared to the clock period. Hence, the power consumption of this architecture will not be significantly higher than the corresponding ungated clock 1024-point FFT architecture. The real strength of this architecture lies in using the optimum FFT length in real time thereby saving power.

## 7. Conclusion

This paper has presented a novel concept of real time adjustment of the FFT size in a wireless receiver as per the channel requirements. A 1-k point reconfigurable FFT processor architecture has been presented which can also act as a 256-point, 64-point and a 16-point processor in real time. This architecture can be very easily modified to support any other combination of sub-carriers. This flexible architecture is ideal under varying channel conditions. The power saving in going down to smaller FFT size is clearly established. This concept of hardware size adjustment on the basis of changing channel parameters can be extended to other receiver blocks like the Viterbi decoder. It is envisaged to design a reconfigurable receiver for MC-CDMA on the basis of the above concepts.

## 8. References

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