

A Novel Low Power Pipelined Architecture for a MC-CDMA receiver

M. Hasan , T. Arslan and John Thompson
School of Engineering and Electronics,
The University of Edinburgh, Edinburgh EH9 3JL, UK
E-mail: mh@ee.ed.ac.uk

Abstract

This paper proposes a novel low power pipelined architecture for a Multi-carrier code division multiple access (MC-CDMA) receiver. The receiver is based on 64 sub-carriers. It comprises of two blocks namely the FFT for demodulation and the combiner for de-spreading and equalization. The 64-point FFT block is based on low power pipelined radix-4 architecture in which coefficient ordering is applied to its second stage to further bring down its power consumption. Clock gating is extensively used in the combiner to reduce its power consumption.

1. Introduction

MC-CDMA [1,2] is a spread spectrum technology which combines the advantages of OFDM (Orthogonal frequency division multiplexing) and CDMA to produce a spectrally efficient multi-user access system. This wireless access system may be utilised in future mobile wireless systems, and hence power consumption is an important issue. A frequency domain processing MC-CDMA receiver contains two main system blocks, a FFT block to demodulate the OFDM signals and a combiner block which equalises the signal and separates out the coded users. The combiner in our architecture is based on MMSE (minimum mean squared error) detection.

It can be shown that the main source of power consumption in a typical CMOS logic gate, is due to the switching power, P_{sw} , given by [3]:

$$P_{sw} = (1/2)kC_{load}V_{dd}^2 f \quad (1)$$

Where V_{dd} is the supply voltage, f is the clock frequency, C_{load} is the load capacitance of the gate, and k is the switching activity factor which is defined as the average number of times the gate makes an active transition in a single clock cycle. Therefore, for achieving low power in CMOS circuits one must target minimising one or more of the parameters C_{load} , V_{dd} and k . This paper deals with low power architectures obtained by reducing the switching activity and also by shutting down blocks through clock gating.

In [4][5], the authors have used the concept of processing data in blocks to reduce the power

consumption in a MC-CDMA receiver. This approach needs a huge amount of RAM in the FFT and hence it is not suitable for the power consuming FFT block. A number of researchers have investigated the area of low power implementation of FFT processors. Work on the application of order based processing to FFT coefficients is restricted. The only reported work involves order based processing of coefficients and data at the inputs of the FFT computational units so as to minimise the overall switching activity of successive coefficients and data samples[7]. This results in coefficient switching activity reduction of just 19% whereas the data activity increases by 1% for a 9-point FFT [7]. The authors in [7] have not shown the actual power reduction obtained by their scheme in the presence of hardware overheads in the full FFT architecture.

This paper proposes low power MC-CDMA receiver architecture. The FFT processor of the receiver is based on a novel coefficient ordered architecture for low power. The combiner block modules are also clock gated to bring down their power consumption.

2. Multi-Carrier CDMA

In MC-CDMA, the user signal is not multiplied by a high speed orthogonal code sequence, but the same bit is transmitted on multiple sub-carriers. The pulse form of each sub-carrier is chosen to ensure orthogonality between sub-carriers. Each sub-carrier is narrowband in nature, so no ISI occurs between successive bits. For each user, the sub-carriers are shifted with a 0 or Π phase offset. The set of sub-carrier phase offsets follows a signature code sequence to distinguish different users. The resulting signal has a coded structure in the frequency domain and multiple access is possible using the orthogonality of the different codes. If the number of sub-carriers is appropriately chosen, then it is highly unlikely that all the sub-carriers will be located in deep fade and hence frequency diversity is achieved. If the processing gain is equal to the number of sub-carriers then this system modulates all the sub-carriers with the same data bit, but with a phase shift on each sub-carrier determined by the spreading code. This multi-carrier modulation can also be implemented using an inverse FFT.

If the k th chip of the spreading code for user u is

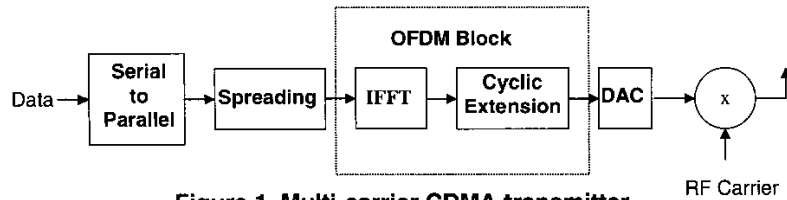


Figure 1. Multi-carrier CDMA transmitter

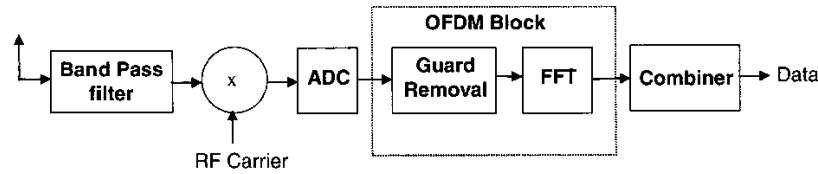


Figure 2. Multi-carrier CDMA receiver

defined as $c(k,u) \in \{-1,+1\}$ then the transmitted baseband signal for the m th data symbol $b(m)$ is:

$$x(n) = \sum_{k=0}^{N-1} \exp(j2\pi kn/N) c(k,u) b(m) \quad (1)$$

The baseband signal is then cyclically extended by more than the channel delay spread to remove ISI. The resulting symbol is then passed through DAC prior to upconversion through the high frequency RF carrier. The block diagram of a MC-CDMA transmitter is shown in Figure 1. By using a guard interval, the receiver selects the portion of the signal that is free from ISI. This is then processed by the FFT block to demodulate the sub-carriers.

The channel effect of a multipath channel $h(n)$ at the output of the FFT is narrowband for each sub-carrier, $H(k)$, and therefore equalisation and despreading can be incorporated into a single combining operation to estimate the transmitted data bit. If the output of the FFT block at frequency bin k is defined as $Y(k)$ then the combining operation can be represented by

$$\hat{x}(n) = \text{sign} \left\{ \sum_{k=0}^{N-1} R\{c(k,u)A(k)Y(k)\} \right\} \quad (2)$$

The entire receiver structure is shown in Figure 2. The combiner block can be implemented by setting $A(k) = H^*(k) / (|H(k)|^2 + \lambda)$ for the minimum mean square error (MMSE) solution, where λ is a parameter

dependent upon the signal to noise level and the number of users.

3. MC-CDMA Receiver Architecture

The basic MC-CDMA receiver consists of a modified pipelined FFT processor and a pipelined combiner. The radix-4 pipelined FFT processor architecture proposed by Bi & Jones [7] has been modified for low power. It is better than other pipelined architectures in terms of computational efficiency and hardware savings in complex multipliers, adders and data stores. The modified architecture is based on altering the ordering of the coefficients fed to the multiplier of the second stage of a 64-point FFT processor so as to minimize the switching activity between successive coefficients resulting in power reduction. The pipelined combiner architecture is also clock gated to reduce the power consumption in its various modules. The two blocks are discussed in detail now

3.1. Modified FFT Processor Architecture

A 64-point modified pipelined radix-4 FFT processor based on [7], shown in Figure 3, has three stages. Each stage produces one output within each word cycle. Each stage contains a commutator (Ci), a butterfly element (Bi for summation) and a complex multiplier, where 'i' indicates the stage number. The

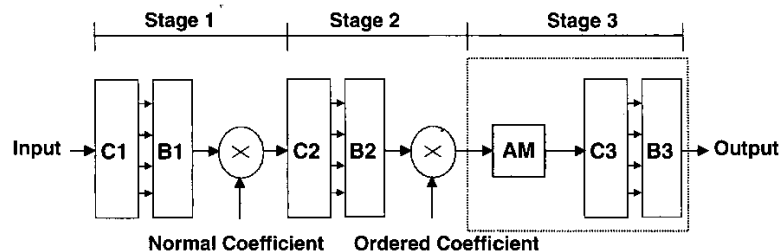


Figure 3. Architecture of 64-point radix-4 pipelined modified FFT processor

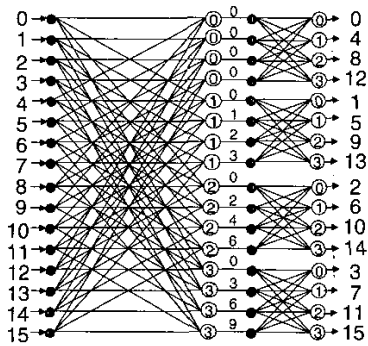


Figure 4. Signal flowgraph of a 16-point radix-4 FFT processor.

sequential outputs at each stage must be ordered in accordance with the circled value m_i in the signal flowgraph shown in Figure 4 for a 16-point radix-4 processor. For instance, from Figure 4; for the 16-point radix-4 processor at stage 1, the outputs associated with $m_1=0$ are produced in the first four word cycles, then those associated with $m_1=1$ in the next four cycles and so on. This paper proposes altered operation sequencing for only stage 1 of a 16-point radix-4 pipelined FFT processor based on Table 1. Normally, the fixed coefficients are fed to the complex multiplier in an order given in Table 1 starting from $m_1 = 0$ and ending with $m_1 = 3$ for stage 1 of a 16-point FFT processor. Our approach involves ordering the coefficient sequence so as to minimise switching activity between successive coefficients fed to the multiplier for stage 1 of a 16-point FFT or stage 2 of a 64-point FFT as listed in Table 1. The coefficients are ordered so as to minimise switching activity between successive coefficients by minimising the Hamming distance between them. The ordered coefficient set is obtained by first arranging only the imaginary part of the coefficient set on the basis of Hamming distance. It is followed by picking up the corresponding real part of the coefficient or its two's complement depending upon the Hamming distance with respect to the previously arranged real part. A flag bit is asserted to indicate the presence of real part in two's complement form. This flag bit is also used to selectively complement the multiplier output [8]. The switching activity decreases from 192 to just 78, a reduction of 59% by following this ordering approach. The coefficient ordering requires corresponding data ordering. The data ordering is performed by a novel design of the commutator for stage 2 of a 64-point radix-4 FFT processor. The ordered data sequence at the output of the complex multiplier for stage 2 of the 64-point FFT processor has to be converted back into a normal data sequence for its stage 3. This data sequence conversion is accomplished by the combination of AM along with a ROM for its addressing as given in Figure 3. The stage 1 and

Table 1. Ordered and normal coefficient sequence for stage 2 of a 64-point FFT processor.

Coefficient sequence after stage 1 of a 16-point FFT	16-bit quantised coefficient sequence (real, Imag)	Ordered sequence	Ordered quantised Coefficient sequence (flag, real, Imag)
W_0	7fff, 0000	W_0	1, 8001, 0000
W_0	7fff, 0000	W_0	1, 8001, 0000
W_0	7fff, 0000	W_0	1, 8001, 0000
W_0	7fff, 0000	W_0	1, 8001, 0000
W_1	7641, cf04	W_0	1, 8001, 0000
W_2	5a82, a57d	W_0	1, 8001, 0000
W_3	30fb, 89be	W_4	0, 0000, 8000
W_0	7fff, 0000	W_1	0, 7641, cf04
W_2	5a82, a57d	W_3	1, cf05, 89be
W_4	0000, 8000	W_3	1, cf05, 89be
W_6	a57d, a57d	W_2	0, 5a82, a57d
W_0	7fff, 0000	W_2	0, 5a82, a57d
W_3	30fb, 89be	W_6	1, 5a83, a57d
W_6	a57d, a57d	W_6	1, 5a83, a57d
W_9	89be, 30fb	W_9	1, 7642, 30fb
Normal Switching activity= 192		Switching activity with ordering = 78	

stage 3 commutators will be the same as given in [7]. It comprises of six shift registers along with three multiplexers. The stage 2 commutator design, to support the ordering scheme, is as follows.

3.1.1. Stage 2 Commutator

As seen in Figure 4, the input data for each summation at stage 1 of a 16-point FFT are separated in time by four words. The timing of the ordered data sequence corresponding to the ordered coefficient sequence and the normal sequence as a function of time is shown in Figure 5, t' is the instant when the first input word arrives. Each input word occupies a

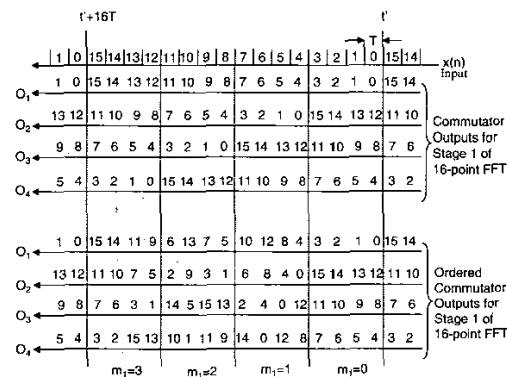


Figure 5. Timing diagram for the ordered and normal commutator outputs of a 16-point FFT processor.

word slot of duration T and is numbered according to its appearance in time. It is difficult to generate the ordered data sequence with the help of a conventional FIFO based commutator as given in [7]. In order to achieve flexibility, this commutator is constructed by using double size (eight words) three triple port RAM (TM) based FIFOs rather than six four word dual port RAM based FIFOs. The additional read port in TM greatly helps in generating the ordered sequence. The commutator comprises of three TMs (Two read ports and one write port), a finite state machine (FSM), a ROM (ROM1) and four multiplexers of variable size as shown in Figure 6. A TM acts as a FIFO with two possible outputs but only four outputs are chosen at any time by the four multiplexers depending upon the desired ordered sequence. Each TM has a depth of eight words for stage 1 of a 16-point FFT processor. The three bit sequential address $a1$ is generated by the FSM of the CONTROL BLOCK for the write ports of $TM0$ and $TM1$ and the B port of $TM0$ respectively. The ROM1 of the CONTROL BLOCK provides the addresses of all the other read and write ports along with multiplexer controls to generate the ordered data sequence. It also helps to keep the unused outputs of TMs to their previous values.

3.2. Pipelined Combiner Architecture

The combiner block performs both de-spreading and equalisation of the FFT outputs to recover the transmitted signal. It carries out equalisation by first estimating the channel transfer function with the help of some known symbols called pilot symbols. The transmitted data is then recovered by dividing the real part of the received signal by the estimated channel transfer function. This method of data recovery is called equalisation.

A MC-CDMA data frame comprises of pilot and data symbols. The pilot symbol helps in estimating the channel transfer function. This transfer function is assumed to remain fixed between two pilot symbols employing linear interpolation. A 64 sub-carrier system is assumed and the data is divided into blocks of 32 symbols, with the first symbol in each block being used as a pilot for channel estimation. The equaliser coefficients corresponding to all the carriers are computed in the estimation phase. These coefficients are stored in the memory and are used in the equalization phase. The equaliser coefficients are assumed to be fixed during the equalisation phase. The pipelined combiner architecture is shown in Figure 7. It comprises of the following modules.

1. De-spreading module.
2. Multiplication and Accumulation module.
3. Division module.
4. Memory module.
5. Finite State Machine (FSM).

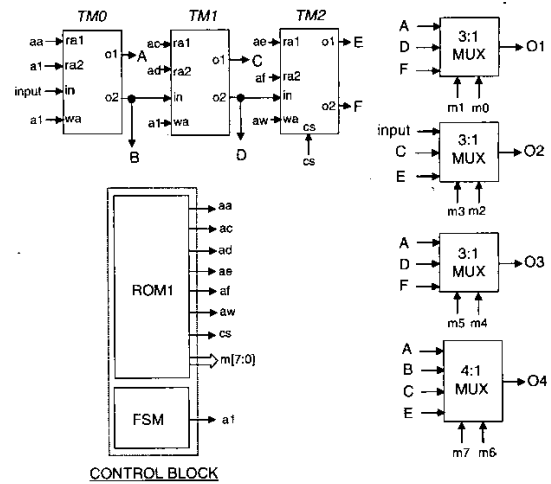


Figure 6. Stage 2 commutator architecture for a 64-point modified FFT processor

3.2.1 De-spreading Module

The main purpose of this module is to multiply the input (FFT outputs) by either +1 or -1 depending upon the corresponding chip value. This is accomplished by selectively complementing the input for chip value of -1 and letting it through for +1. This task can be performed easily by a set of XOR gates with one of their input connected to the chip value. The chip values are stored in a 64-bit ROM.

3.2.2. Multiplication and Accumulation Module

This module comprises of two multipliers which are used both in the channel estimation phase as well as in the equalisation phase for reducing power consumption as shown in Figure 8. In the channel estimation phase, the multipliers Mult I and Mult II are fed with the same input x_r and x_i respectively. This is accomplished by controlling the select inputs S_{11} and S_{12} of MUX A and MUX B with the help of a FSM. The control input S_{13} is set to '0' in the estimation phase so that the summation of the two multiplier outputs is performed by the summer (SUM). The summer based accumulator is used

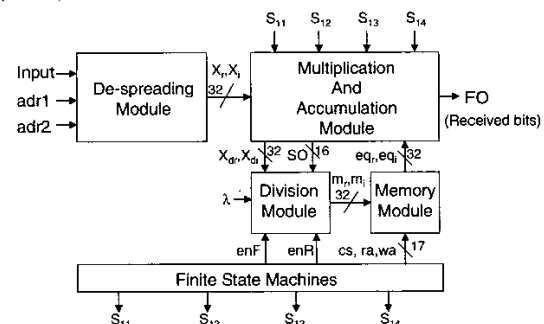


Figure 7. Pipelined Combiner Architecture

instead of a programmable adder/subtractor to reduce the power consumption. The select input S_{14} in the estimation phase always selects '0' for summing the two multiplier outputs. The output so (the square of the channel transfer function $(x_r^2 + x_i^2)$) from this module feeds into the division module for computation of the equaliser coefficients. The registers are used at the input of the multipliers to reduce the input switching activity and hence the power consumption. Moreover, registers between the summer and the multiplier are used for reducing the length of the critical path and hence low power consumption on account of less buffering.

The equalisation phase requires the calculation of the real part of the product of data and the equaliser coefficient $(x_r \cdot eq_r - x_i \cdot eq_i)$ for each sub-carrier followed by their summation over all the sub-carriers. The multiplier Mult I is fed with x_r and eq_r and Mult II with x_i and eq_i . This is again controlled by the select lines S_{11} and S_{12} in Figure 8. The XOR control input S_{13} is set to '1' in the equalisation phase to compute the difference between the two multiplier outputs by the summer. The select input S_{14} in the equalisation phase is set such that it selects zero input corresponding to the first data sub-carrier and accumulator output (ACC) for the rest of the data sub-carriers. The MSB of the accumulated output (FO) is a measure of the transmitted bit. The outputs xd_r and xd_i are fed to the division module to reduce the size of FIFO by one register level.

3.2.3. Division Module

The division module is used to compute the real and imaginary parts of the equaliser coefficients m_r and m_i respectively by using the input pilot symbol and so input from the Accumulation module and is shown in Figure 9. The real part of the equaliser coefficient m_r is obtained by dividing the real part of the pilot symbol with the summation of so (square of channel transfer function) and the factor λ . The imaginary part of the equaliser coefficient is obtained by dividing the complement of the imaginary part of the pilot symbol with the previous divisor. The negation of the imaginary part is done to obtain the equaliser coefficient tending towards the reciprocal of the channel transfer function. This is required to remove the channel effects later by multiplying the incoming data block with the equaliser coefficients.

The Two word FIFO block and the register (R) are enabled only during the channel estimation phase by enF and enR signals. This helps in reducing the power consumption by reducing the switching activity at the divider inputs and inside the FIFO block. The FIFO is needed to synchronise the numerator and the denominator of the Divisor. A 1's complemeter block (COMP) is also needed to generate the complement of the imaginary part of the FIFO output. The division

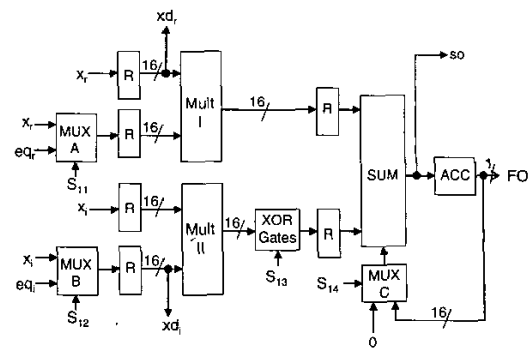


Figure 8. Multiplication and Accumulation Module

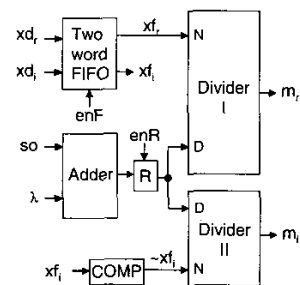


Figure 9. Division Module

module does not consume much power because it is active only during the short channel estimation phases. Hence, the design is based on two dividers namely Divider I and Divider II with 'N' indicating numerator and 'D' for denominator.

3.2.4. Memory Module

The memory module is used to store the equaliser coefficients. The memory size required in a 64 sub-carrier system is 64-words. The dual port RAM is used because of the need of simultaneous read and write operation due to slight overlap of the channel estimation and equalisation phases in the receiver.

3.2.5. Finite State Machines Module

The Finite state machine in Figure 7 generates 23 control signals. The control signals S_{11} , S_{12} , S_{13} and S_{14} controls the blocks in the Multiplication and Accumulation module whereas enable signals enF and enR controls the selective enabling of blocks in the Division module. It also generates the read address (ra) and write address (wa) for the dual port RAM.

4. Results

The MC-CDMA receiver core has been designed at the register transfer level (RTL) using Verilog

Table 2. Total Receiver Power Consumption

Major cells of the Receiver	Cell Power consumption (mW)
FFT	89.78
Combiner	29.04
Total receiver cell power consumption(Cell+net)	126.75 (118.82 + 7.93)

Table 3. Power consumed by the major cells of the FFT.

Major cells of the FFT	Power consumption (mW)
First Stage Commutator	41.74
Second Stage Commutator	13.56
Third Stage Commutator	8.26
First Stage Multiplier	11.00
Second Stage Multiplier	7.13
Butterfly	1.6

Table 4. Power consumed by the major cells of the combiner.

Major cells of the Combiner	Cell Power consumption (mW)
Multiplier	2.13
Summer	0.28
FIFO	0.74
Divider	0.30
Memory	19.68

hardware description language. The core was then synthesized using SYNOPSIS *DesignCompiler* with UMC 0.18 μ standard cell CMOS library. A layout of the core was generated using *EnvisaTM Silicon EnsembleTM* place-and-route software. This was followed by extracting RC information and then performing RC back-annotated post layout gate-level netlist simulations for 4000 uniformly distributed random input data samples using Verilog-XLTM simulator. The resulting data including switching activity of the circuit nets and capacitive load information extracted from the layout was then used by the Synopsys *DesignPower* to compute the power consumption of the receiver. All the simulations are carried out at a clock frequency of 50MHz. The results are listed in Tables 2, 3 and 4. The total power consumed by the receiver is around 126.75 mW. The additional 7.93mW of power in Table 2 is consumed by the switching of the Input/output nets. The power consumed by the FFT cell is much more than the power consumed by the combiner cell as per Table 2. It is evident from Table 3 that the stage 1 commutator consumes most of the power in the FFT. The power consumed by the stage 2 multiplier is less than stage 1

multiplier because coefficient ordering is only applied to stage 2 of the 64-point FFT. It is clear from Table 4 that the memory consumes most of the power in the combiner cell. Moreover, the power consumed by the divider cell is much less than the multiplier in the combiner cell because the divider is active only during the estimation phase and not in the equalization phase.

5. Conclusion

MC-CDMA based architectures are deemed to be crucial in future mobile systems. This paper has presented low power receiver architecture. Techniques like coefficient ordering and clock gating have been employed selectively within the various blocks of the receiver providing an overall power reduction for the whole receiver.

6. References

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