

A TRIPLE PORT RAM BASED LOW POWER COMMUTATOR ARCHITECTURE FOR A PIPELINED FFT PROCESSOR

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ABSTRACT

This paper proposes a low power commutator architecture based on triple port RAMs rather than dual port RAMs or conventional FIFO for the radix-4 pipelined FFT processor implementation. The triple port RAM based commutator consumes less power than the other two for the first and second stages of a 64-point radix-4 pipelined FFT processor. This commutator is attractive for shorter FFT's but can also be used in the last stages of longer FFT's. Up to 29% and 9% power savings is achieved for the 8-12 bit data range in the second and first stages of a 64-point FFT processor respectively.

1. INTRODUCTION

One of the fastest growing areas in the computing industry is the provision of high throughput DSP and Telecommunication systems in portable forms. With the advent of SoC (Silicon on chip) technology, DSP algorithms such as Fast Fourier Transform (FFT) are being prototyped as parameterisable cores which could be embedded within the SoC platform. For high performance low power applications like multicarrier systems, there is a continuous demand for FFT/IFFT cores [1][2], which provide high throughput while minimising power consumption.

It can be shown that the main source of power consumption in a typical CMOS logic gate, is due to switching power, P_{sw} , given by [3]:

$$P_{sw} = \frac{1}{2} k \cdot C_{load} V_{dd}^2 f \quad (1)$$

Where V_{dd} is the supply voltage, f is the clock frequency, C_{load} is the load capacitance of the gate, and 'k' is the switching activity factor which is defined as the average number of times the gate makes an active transition in a single clock cycle. Therefore, for achieving low power in CMOS circuits one must target minimising one or more of the parameters C_{load} , V_{dd} and k . This paper primarily deals with low power architectures obtained by reducing the switching activity. The paper presents an architecture for

realising a low power commutator for a radix-4 pipelined FFT processor. This commutator is attractive for shorter FFT's but can be used in the last stages of longer FFT's as well.

2. ALGORITHM

The N-point DFT of a finite duration sequence $x(n)$ is defined by

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \quad k = 0, 1, \dots, N-1; \quad (2)$$

$$\text{where } W_N = e^{-j(2\pi/N)}$$

For radix r_1 , equation 2 can be written as follows.

$$X(k) = \sum_{q_1=0}^{N_1-1} W_N^{q_1 k} \sum_{p=0}^{r_1-1} x(N_1 p + q_1) W_{r_1}^{pk} \quad (3)$$

The N-point DFT described by (3) can be decomposed into v stages where $N = r_1 r_2 \dots r_v$ from [4]. The final stage is defined by

$$X(r_1 r_2 \dots r_{v-1} m_v + \dots + r_1 m_2 + m_1) = \sum_{q_{v-1}=0}^{r_v-1} x_{v-1}(q_{v-1}, m_{v-1}) W_{r_v}^{q_{v-1} m_v} \dots \quad (4)$$

while intermediate stages (t) are given by the recursive equation as follows.

$$x_t(q_t, m_t) = W_{N_{t-1}}^{q_t m_t} \sum_{p=0}^{r_t-1} x_{t-1}(N_{t-1} p + q_t, m_{t-1}) W_{r_t}^{p m_t}$$

$$2 \leq t \leq v-1, 0 \leq m_t \leq r_t-1, 0 \leq q_t \leq r_t-1$$

For $r_1 = 4$, the flowgraph of a 16-point FFT based on the above formulation is shown in Figure 1. The corresponding equations are as follows.

$$X(4m_2 + m_1) = \sum_{q_1=0}^3 x_1(q_1, m_1) W_4^{q_1 m_2}$$

$$x_1(q_1, m_1) = W_{16}^{q_1 m_1} \sum_{p=0}^3 x_0(4p + q_1) W_4^{p m_1} \quad 0 \leq m_1, m_2 \leq 3$$

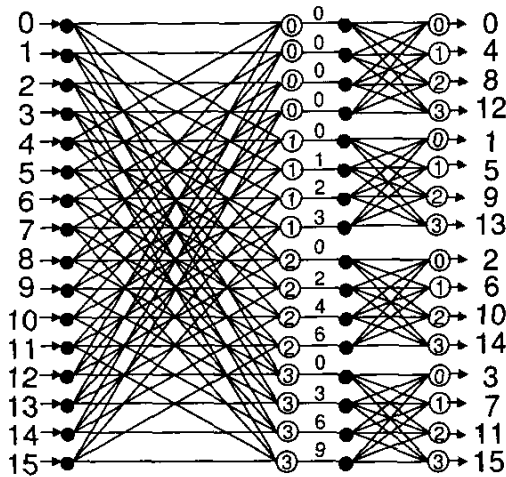


Figure 1: Signal flowgraph of a radix-4 16-point FFT

In figure 1, each open circle represents the summation while the dots define the stage boundaries. The number inside the open circle is the value of m_1 (for the first stage) or m_2 (for the second stage). The number outside the open circle is the twiddle factor applied. From equation (3), it is clear that the input data for each summation at stage t are separated in time by N_t words. The commutator structure to realize N_t word separation is shown in Figure 2 [4]. It is based on six N_t length FIFO's along with three multiplexers. The select lines of the multiplexers are dependent on the values of m_t . The FIFO block within the commutator structure can be realised in many ways. The conventional method is to realise this FIFO by using a shift register. In this method, each FIFO block in Figure 2 is replaced by N_t word shift registers. This results in an architecture similar to Figure 2 called here as *SR*. In the second method, each FIFO block is realised using a dual port RAM (DM) along with a register leading to a commutator architecture termed here *DR*. In this paper, we have proposed a novel triple port RAM (TM) based commutator architecture *TR* in which three FIFO blocks of size $2N_t$ are used instead of six FIFO blocks of size N_t . This architecture, shown in Figure 3, realises FIFO of size $2N_t$ by using a $2N_t$ word triple port RAM along with a register. The use of larger RAMs results in less data movement as compared to other architectures and hence more power savings.

3. IMPLEMENTATION

The TM based FIFO is constructed by controlling the read and write addresses namely ra_1 , ra_2 and wa respectively as shown in Figure 3. These addresses are manipulated with the help of a finite state machine (FSM) and the ROM of

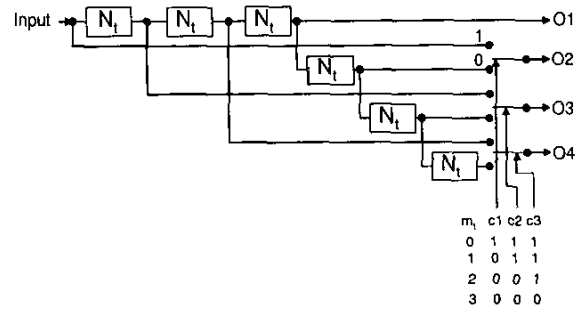


Figure 2: General commutator architecture for the radix-4 pipelined FFT processor

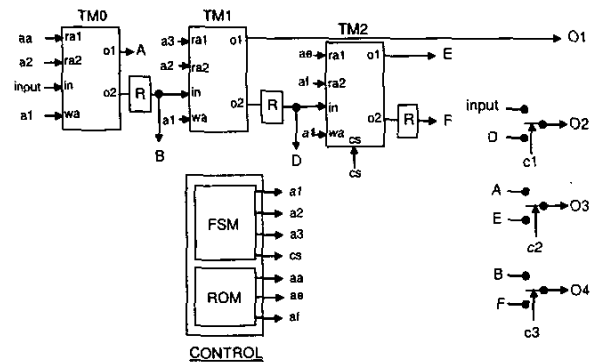


Figure 3: TM based Commutator architecture *TR* for the pipelined FFT processor

the CONTROL block depending upon the required data. The operation of *TR* architecture can be understood with the help of the timing diagram shown in Figure 4 for the first stage commutator of a 16-point radix-4 FFT processor as an example, where 't' is the instant when the first input word arrives. Each input word occupies a word slot of duration T and is numbered according to its appearance in time. The desired output sequence shown in Figure 5 is dependent on the values of m_1 for this architecture. The TM output sequences (A, B, C, D, E and F) are obtained by controlling the read and write addresses of all the TM's depending upon the value of m_1 . The desired four output sequences (O_1 , O_2 , O_3 and O_4) are then obtained by controlling the selection lines of the multiplexer as per m_1 . The TM outputs are allowed to switch only if their values are currently required. Only four outputs are required at any given time out of a total of six possible outputs. The unused outputs are maintained at their previous values to reduce unnecessary switching activity. An additional ROM in the CONTROL block is

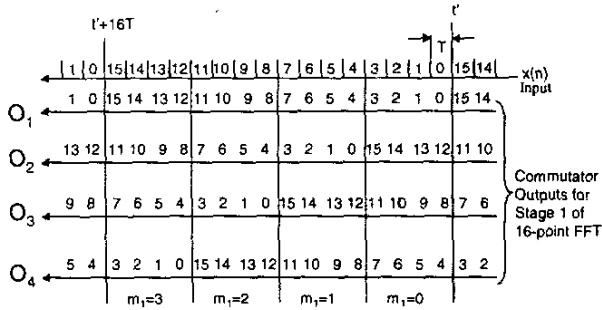


Figure 4: Timing diagram of Commutator outputs for the first stage of a 16-point FFT processor.

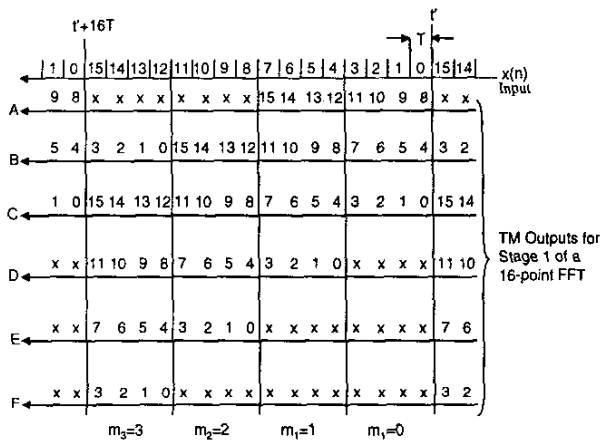


Figure 5: Timing diagram of TM outputs for the first stage of a 16-point FFT processor

required to generate RAM addresses such that the unused outputs are maintained at their previous values for least switching activity. The chip select input of TM2 is also selectively disabled by the CONTROL block based FSM for writing operation during $m_1=0$ and $m_1=3$. The outputs of TM indicated as 'x' are not required and hence must be maintained at their previous values by addressing through the ROM.

The TR architecture for the first stage of a 16-point FFT processor requires three TMs each having eight locations. The three bit addresses a1, a2 and a3 corresponding to the write port and read ports B and C are generated through the FSM. The write address a1 and the read address a2 are displaced by one location to realise a FIFO with the help

of a RAM and a register. The second read address a3 is displaced by four locations with respect to a1 to track the data entered four clock cycles earlier. The other three addresses aa, ae and af are generated by the ROM. The ROM based address generation is required to keep the unused outputs of ports A, E and F at their previous values for less switching activity. The power consumption in CMOS is a strong function of switching activity. In TR architecture, the data movement and hence switching activity between RAMs is reduced by using smaller number of bigger size RAMs. Moreover, the switching activity at the unused ports is kept to a minimum by maintaining their outputs to their previous values by addressing through the ROM. This approach leads to power savings only in the first and second stage commutators of a 64-point pipelined radix-4 FFT processor. It has been observed that this architecture is not attractive for RAMs larger than 32*32 words long due to the higher power consumption in the additional port needed in TM as compared to DM. However, this architecture can be effectively used in the last stages of longer FFTs.

4. SIMULATION RESULTS

The three architectures namely SR, DR and TR have been implemented in register transfer level Verilog hardware description language for different bit lengths and then synthesized using Synopsys DesignCompiler with 0.35u Alcatel MTC45000 CMOS technology library. Power evaluation was carried out using Synopsys DesignPower for the circuit netlist for 20,000 clock cycles using a supply voltage of 3.3V and a clock frequency of 10 MHz.

The comparative results in terms of power reduction for the different bit lengths and FFT stages are given in Figure 6 and Figure 7. It is clear from these figures that Our TR commutator architecture is much better than both SR and DR in terms of power consumption for the first and second commutator stages of the radix-4 pipelined FFT processor. Our TR architecture gives power savings in the range of 23-29% for the most commonly used 8-12 bit range relative to SR for the first stage of the 64-point FFT processor. It also achieves power savings in the range of 4-9% for the same bit range relative to DR for the same stage. For the second 64-point FFT stage, the power saving relative to DR and SR are in the range of 26-27% and 17-21% respectively for the same bit range.

The power savings of TR relative to SR is slightly less for longer bit lengths on account of the fact that the port switching power in the TR has gone up considerably with the bit length. Hence, maximum power savings is obtained for shorter bit lengths relative to SR. The power savings is

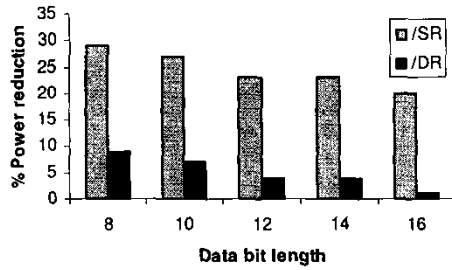


Figure 6: Power comparison of *TR* relative to *SR* and *DR* for the first stage of a 64-point FFT processor.

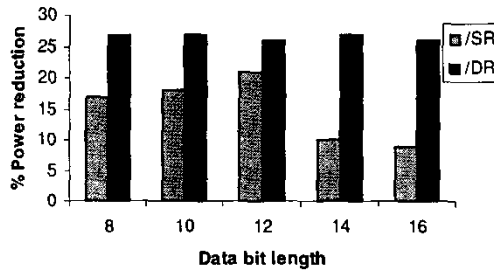


Figure 7: Power comparison of *TR* relative to *SR* and *DR* for the second stage of a 64-point FFT processor.

very low for longer bit lengths for the first FFT stage relative to *DR* because the power consumption in the additional port required by *TR* increases considerably on account of the requirement of bigger RAMs for this stage

as compared to the second stage. The power savings is higher relative to *SR* in the first stage because the switching power in *SR* also increases sharply with the FIFO size.

5. CONCLUSION

This paper has presented a novel low power commutator architecture based on triple port RAMs rather than dual port RAMs for a low power pipelined radix-4 FFT processor. This low power commutator architecture gives power savings for shorter FFTs up to 64-points. This architecture is also suitable for the design of the last stages of longer FFTs requiring smaller size RAMs.

6. REFERENCES

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