Low Power Macro Component Library Framework for the Design and Verification of DSP IPs for Hearing Aid Applications

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1. Abstract

The aim of this work is the development of macro components for the rapid design and verification of DSP system IPs for hearing aid applications. Hearing aid devices have challenging power and area requirements due to the small battery capacitance and limited volume. For this reason the macro components are specified tailored for low power operation. A unified power reduction strategy is employed in the design of the library which targets the reduction of dynamic switching power of the complete IP system through reduction in the amount of switched capacitance within its constituent components. Individual macro components are associated with dedicated BIST circuitry, for blocks such as memory or MAC, which maintain low power features while achieving high fault coverage. The library framework comprises of components, component generators and verification units developed in an environment which could utilise different synthesis, verification and testbenching tools.

Keywords: *Low Power, IP framework, Digital Filter, Design for Testability (DfT)*

2. Motivation

The advent of digital signal processing in hearing aids has made low power circuit design an increasingly important research area. The requirements of a digital hearing aid regarding power and area consumption are amongst the strictest looking at portable devices.
The work on digital signal processing for hearing aid applications reported in the past is either based on a full customised design of the processor including DSP core [1] [2] or makes use of a generic DSP core [3]. Products available on the market today are all based on customized DSP cores because the power dissipation of generic cores is not acceptable yet.
The work presented from Neuteboom et.all. [1] and Moller et. all. [2] does not look into the details of the integration despite of the multiply-accumulate (MAC) units.
Our investigations in digital filter design for hearing aid applications show that it is well worth looking at the overall architecture in greater detail.
If we look at Eq. 1 which describes an FIR Filter and draw a block diagram of the filter it can be seen that a few major components can be isolated from the diagram.

$$y_n = \sum_{m=0}^{M-1} b_m \cdot x_{n-m} \qquad \text{Eq. 1}$$

A multiply-add element, the basis of every filter and several forms of memory such as for the sample values x_{n-m} and the coefficient values b_m can be isolated. A storage cell for the filter output value y_n is required and a control function which schedules the different modules. The basic building blocks of an FIR filter are therefore:

- Coefficient memory
- Input data sample memory
- Multiply-accumulate unit (MAC)
- Output storage
- Controller

Figure 2-1 illustrates the principle data flow between these components in a block diagram.

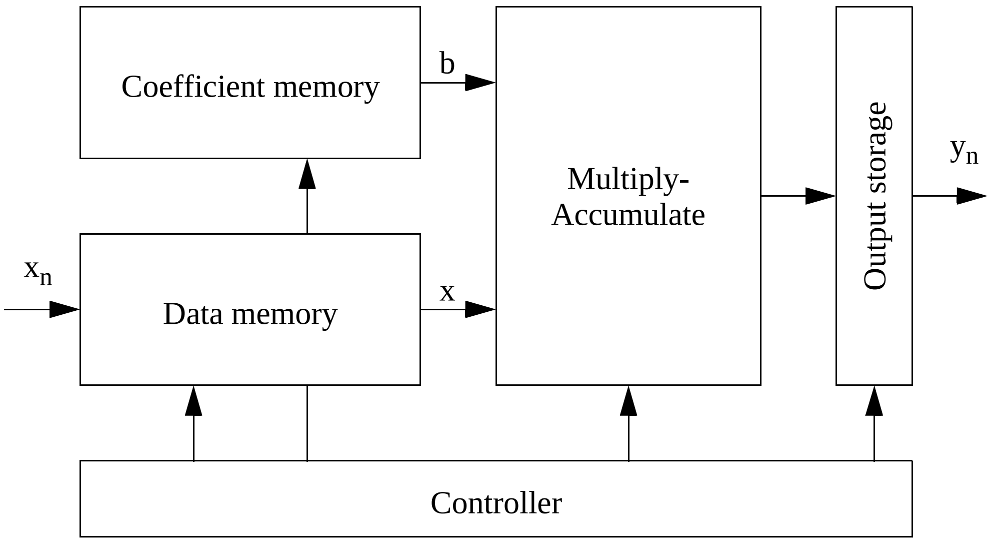

Figure 2-1 System Architecture of FIR Filter

When analysing other Filters (e.g. IIR, Lattice) or Fast Fourier Transform (FFT) modules the same components can be isolated too.
It would therefore be very helpful for a designer to have a library available where such components can be taken from. This paper proposes the integration of such a library with the following requirements:

- Low power dissipation
- Low area consumption
- Flexibility through use of HDL (including synthesisability)
- Parametrisability
- Design for Testability (DfT)

The components can not only be used for the design of macro units, but also for the design of complete filter structures and hearing aid applications. We propose to make both small and big components available to designers.
The designer makes use of this library as an Intellectual Property (IP) and it is very important that DfT aspects are not ignored when implementing this components with regard to the final use of these components in hearing aid applications. The next chapter gives an overview of the integrated macro components.

3. Macro component library

We have analysed and implemented different filter types and defined a set of cells. These cells have then be categorised and verified. The following categories of components have been defined from the implemented cells:

- Clock (e.g. clock gate)
- Counter
- Multiplexer
- Memory, Storage
- Arithmetic
- Decision
- Conversion
- DfT

The first category which has been defined are clock related cells. The strong requirements of the macro components regarding power dissipation can only be achieved by using gated clock whenever possible. Clock gate cells for different clock gate methods have therefore been implemented.
We added global enable signal to sequential macro components where applicable with which the clock of the individual cell is gated. The individual component will only dissipate power if it is enabled and the area is also reduced due to the simplified functionality. The proposed scheme is illustrated in Figure 3-1.

Verilog HDL description

conventional

```
1   always @(posedge clock)
2   begin
3     if (enable)
4       state <= #1 new_state;
5     else
6       state <= #1 state;
7   end
```

low power

```
1   always @(negedge clock)
2   begin
3     clock_ena <= #1 enable;
4   end
5
6   g_clock = clock && clock_ena;
7
8   always @(posedge g_clock)
9   begin
10    state <= #1 new_state;
11  end
```

Figure 3-1 Low power Verilog description

These macro component cells will therefore only dissipate power if they are enabled. This is achieved using clock-gating (see Line 8 of low power description) and the required area is reduced due to a simpler logic because no *else* statement is necessary (see Line 6 of conventional description).
A basic set of parametrisable counters with options such as gated clock, enable, up respectively down counting and scan path are also available.
Strong emphasis has been put on the design of multiplexer and demultiplexer with focus on small area usage, low power dissipation and design for testability. We compared the discrete multiplexer structure [4] with a new design low power multiplexer and a sea-of-gate type multiplexer. Our low power multiplexer is using a special address decoder generating individual enable signal for every multiplexer leave to reduce the toggle activity. A sea-of-gate multiplexer

is implemented using the Verilog *casex* construct for address decoding and automatic synthesis tools.
The design of multiplexer and demultiplexer is especially important because they are also the building blocks of memories. Figure 3-2 illustrates the block diagram of a RAM cell. Small sizes of RAM, as they are often used in filters are not built from vendor megacells, in particular in hearing aid applications.

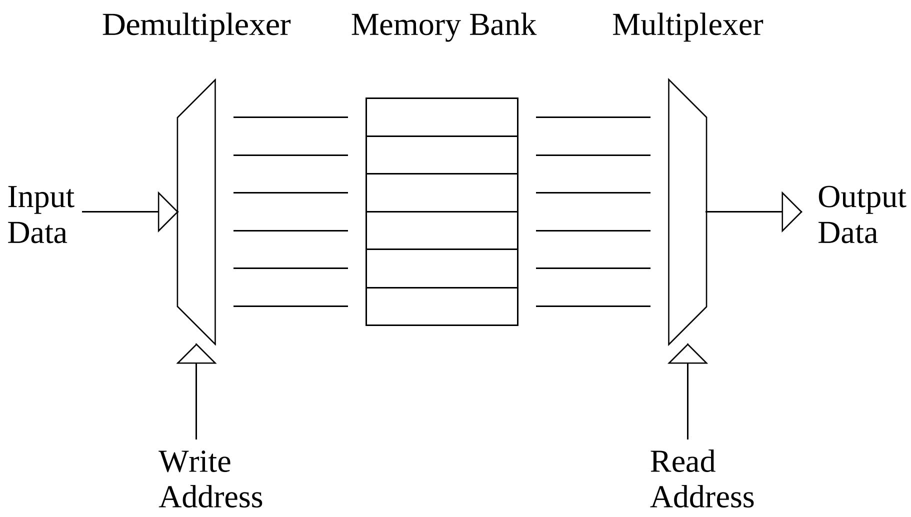

Figure 3-2 Block diagram of memory cell (RAM)

The demultiplexer and the multiplexer are major building blocks of the memory cells and it is helpful to have a set of different sizes available for building different sizes of memory. We therefore developed a multitude of different generator cells using a behavioral Verilog description which, after setting several parameters, generate a RTL Verilog description of for example a multiplexer or demultiplexer.
Another set of major building blocks are arithmetic components. Functions like increment, add, multiply, and multiply-accumulate are used very often in digital filters. Special attention has been given to the development of multipliers and multiply-accumulators, where different principles like those suggested by Dadda, Wallace and Booth [5] have been implemented and verified.
Hearing aid applications also require functions such as Min(a,b) or Equal(a,b) which have been assembled in a category named *decision* and other function like y=Round(a) or y=Shift(a,n) which have been put into a category named *conversion*.
Pattern generators (e.g. RAM BIST [8]) and data compressors (e.g. BIST signature) cells have been implemented following a strict low power policy and included into the DfT category of the macro component library.
FIR Filters where then built using the available components and it came clear soon that the development time could be drastically reduced with the use of the macro component library as development of the filter is reduced to picking the right components, connecting them together and designing the controller.

One aim of the design of the components is not to add an extensive set of cells with different size and width but to add parameterisability wherever possible. Complex cells with high repetition of code shall not be part of the library. A generator cell is then added with which any cell with variable width and depth can be generated.

Another advantage of the component library is that it can grow constantly and new know-how (e.g. new low power method) has to be added only at one place.

4. IP framework

The individual macro component cell will only be released and made available in the library if its functionality has been carefully verified. Two criteria, amongst low area usage and low power dissipation, have to be distinguished. These are:

- Functionality
- Fault coverage

The proper functionality has to be guaranteed to fulfil the specification and an acceptable fault coverage has to be achieved for manufacturing. The test versus verification process is illustrated in Figure 4-1.

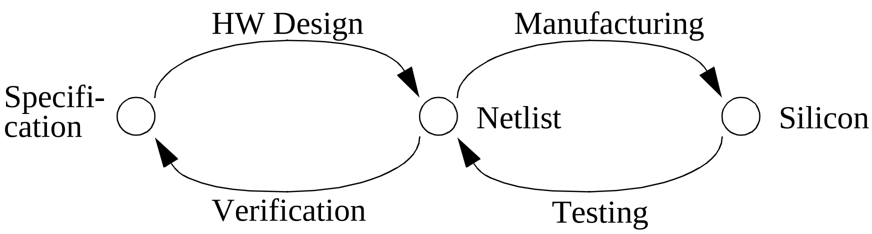

Figure 4-1 Testing vs. Verification [9]

Low power dissipation and area usage is analysed after the functionality has been verified and the testability is guaranteed.

4.1 Verification

The macro components are verified on different integration levels. We propose to start designing a new cell by writing a high-level model of the required functionality. For signal processing applications we found Matlab a very convenient tool.
Once the Matlab model has been properly verified a functional[1] Verilog model can be developed. The functional model is verified using the generated input stimuli from the Matlab simulation and the output response is compared.
It is necessary to choose a technology to further analyse the implemented cells regarding area usage and power dissipation. The RTL model of the different cells can then be synthesised and the input stimuli is used for checking the proper functionality. The netlist simulation is further used for generating a switching activity report with which the power dissipation can be estimated using a power analysis tool. Figure 4-2 illustrates the verification process.

1. We refer to a functional Verilog model as an synthesisable RTL (Register Transfer Level) description of a cell.

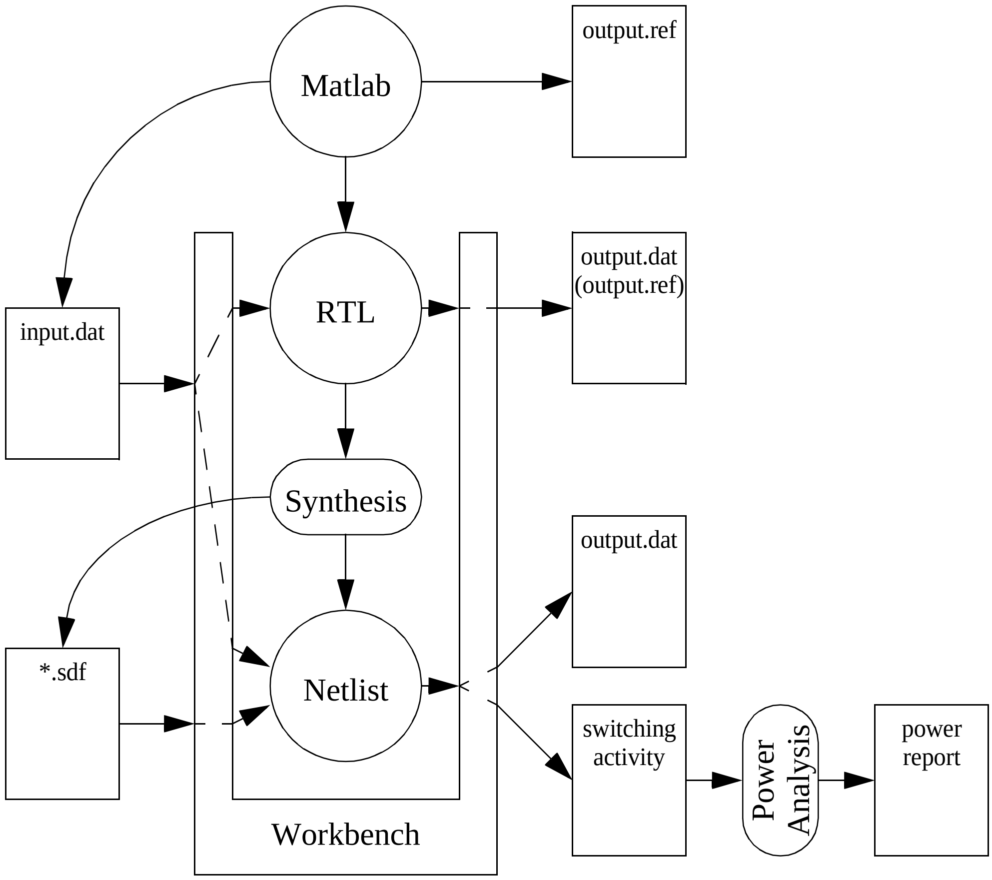

Figure 4-2 Verification process of the macro components

The proposed verification process is used to qualify the low area usage and power dissipation of simple macro component cells like counters or multiplexer, of complex memory cells and complete filter structures. Two different input signals have been used for the verification, those are:

- Random input data (White noise, $\mu = 0$, $\sigma = 0.5$)[1]
- Typical filter data (Noisy sine, $f = f_s/5$, $s/n = 1$)[2]

The verification of general purpose cells is best done with random input data while the power dissipation of multiplexer has been analysed with both random signal and typical filter data. The filters have been verified with typical filter data.

4.2 Test

If the functional verification is passed the different components also need to be checked for their Design for Testability (DfT). Figure 4-3 illustrates the test process used for checking the fault coverage and testability of the macro components cells and IPs.

1. μ is the mean value and σ is the standard deviation
2. f is the signal frequency, f_s is the sample frequency and *s/n* is the signal to noise ratio

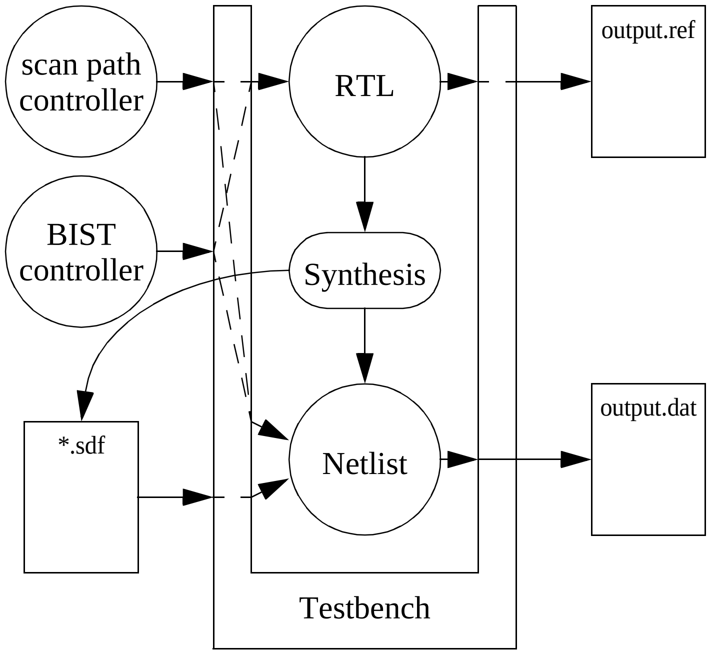

Figure 4-3 Test process of the macro components

The required fault coverage of the macro components is achieved using scan path and Built-In Self-Test (BIST). Both the scan path and BIST controller are not integrated in a hearing aid application due to the strict area requirements. The test machine is therefore completing the required processing and models of the two controllers are used for checking the testability of the macro components and IPs.

5. Results

A macro component library framework for the design and verification of DSP IPs in hearing aid applications has been implemented using the proposed design and verification flow. First a Matlab model of a component has been generated and thoroughly tested. The input stimuli and output response were then used for verifying the Verilog HDL description and the synthesised netlist of the macro component. Different circuit structures and architectures have been analysed regarding area usage, circuit delay, power dissipation and fault coverage.
Our investigations included different multiplier and MAC circuits and we have compared Dadda, Wallace and Booth multipliers [5] with the proposed pBooth multiplier [2], which was specially designed for hearing aid applications. Different number formats [6] such as 2's complement, sign & magnitude, and redundant signed-digit have been used for the implementation of these multipliers.
Pre-computation [7] circuits have also been analysed with special emphasis laid on the comparison of sequential and combinatorial circuits. We found that most of the power of implemented cells such as y = Min(a,b) is dissipated in the register and only a small portion in the arithmetic logic itself. Our test have shown that the increased power dissipation due to glitches when using blocking-logic still leads to overall power savings.
A multitude of FIR filters where then built and analysed using the designed macro components. The proposed verification and test process have been used successfully.

6. Conclusions

The proposed low power macro component library framework for the design and verification of DSP IPs for hearing aid applications has been successfully verified. The macro component library will be a constant source of good designs work if it is modified and maintained on a regular basis and the library framework and the verification and test process are very helpful and result in a faster design cycle without lacking important integration features such as DfT.

7. Acknowledgements

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