

Low power multi-segment sequential one hot addressing architecture

K.-C.B. Tan and T. Arslan

Abstract: Sequential addressing is one of the essential power-consuming parts of digital signal processing (DSP), which is mainly used for sequential memory and coefficient selection. The use of sequential addressing is not only widespread, but also particularly important in a wide variety of DSP applications as most of the computation process proceeds in a sequential manner. Therefore, by reducing both the power of the sequential memory addressing hardware and accesses within the DSP system, the overall power consumption of the system will be effectively reduced. A novel scalable low power multi-segment one-hot all-sequential addressing architecture (MSML-OHA) is presented. This architecture, implemented in 0.18 μm CMOS technology, reduces power dissipation by more than 20% compared to conventional counter-decoder architecture.

1 Introduction

High-speed, low-level, essential and repetitive sequential tasks in high throughput DSP systems are often the parts of the system that consume a considerable amount of power. One such essential power-consuming component of a DSP system is the address decoder or local addressing logic, which is used mainly for sequential memory selection. So far, no one has targeted their research into reducing internal power consumption of local addressing or in the address decoder of a VLSI system, through switching area reduction and architecture optimisation. Most low power research work to date only considered reducing switching activity [1–4] on the address bus by some means of bus coding. These techniques seek to reduce power consumption in transmitting addressing information from one part of a system to another part, and assume that there are considerable amounts of capacitance on these buses. For example the work in [1–3] was aimed at reducing power on an off-chip address bus by modifying and utilising transition coding. One of the most simple and popular coding methods is Gray coding (see [1]). Most of these techniques do not take into consideration the internal switching of the addressing logic and the additional hardware overhead that contribute to the overall power consumption of the system.

In this paper, a novel scalable sequential multi-segment multi-level one-hot addressing architecture (MSML-OHA) is proposed to reduce internal local all-sequential addressing power consumption. The architecture is made up of chains of one-hot shift registers segments and a combinational logic network for the final output selection. This architecture saves power by more than 20% over conventional

counter-decoder architecture and it can be used as part of any low power system.

2 Sequentially addressed memory

A computing and digital processing system utilises sequentially addressed memory or sequential addressing in one form or another. The use of sequential addressing can be seen in first-in-first-out (FIFO) memory, ring buffer memory and coefficients pointer. Sequential addressing is not only widespread, but also particularly important in a wide variety of digital signal processing applications where most of its computation process proceeds in a sequential manner. As the majority of DSP systems involve computation in a sequential manner, the overall power consumption of the system can be reduced effectively if both the power of the memory addressing hardware and accesses within the DSP system are reduced.

2.1 Conventional sequential addressing hardware

Conventionally, sequential addressing logic is built from two main components; the up-counter and the decoder (see Fig. 1). The up-counter provides the sequentially incremental address whereas the decoder decodes the address into individual select-enable signals. The up-counter can either be a binary counter or a Gray code counter. This architecture is commonly used in digital systems for sequential addressing in addition to random addressing to some extent. The up-counter and the decoder can be categorised broadly into two logic group types. The up-counter is categorised as register-memory logic and the decoder as combinational logic. By simply clocking the up-counter, this design will be able to address sequentially. This simple conventional counter-decoder architecture (CCD) is relatively power efficient and easy to build when the depth sizes (size of address space) are small. However, when this architecture is scaled up, it is no longer power efficient. This is because as the counter size and the depth size increase, the number of gates in the combinational logic portion of the CCD increases exponentially. As a result of this increase in the number of combinational gates, the total amount of switching activities of the system is also increased. This is

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K.-C.B. Tan is with Fujitsu Microelectronics Asia Pte Ltd., 151 Lorong Chuan, New Tech Park, 05-08, Singapore 556741

T. Arslan is with Institute of Integrated Micro and Nano Systems, School of Engineering and Electronics, The University of Edinburgh, The King's Buildings, Mayfield Road, Edinburgh, EH9 3JL, Scotland, UK

E-mail: benny.tan@fmal.fujitsu.com

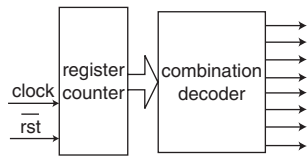


Fig. 1 Conventional counter-decoder (CCD) architecture

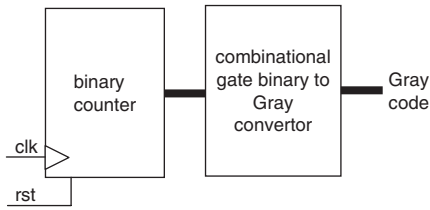


Fig. 2 Conventional binary to Gray code counter implementation

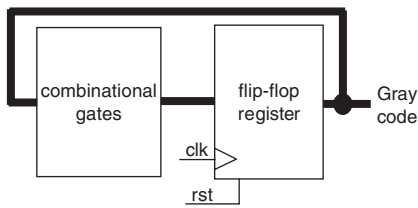


Fig. 3 Native pre-modification Gray counter

due to the fact that switching signals from the counter would have to ripple through an increased number of gates before reaching the outputs. Such lengthening of the switching paths not only increases the power consumption of the system, it also increases the signal propagation delay. Therefore, alternative architectures were examined to try to minimise the power consumed by the sequential addressing hardware. One of the commonly used low power architectures is the Gray code counter-decoder (GCCD). The architecture design and implementation of all Gray code decoders is the same as binary decoders except that the output positions of a Gray decoder are different from those of a binary decoder. There are in existence three implementation variations of the GCCD. The three variations of GCCD are only different in the design of Gray counter. The first variation of GCCD is the most commonly used simple binary to Gray code (post-modification) counter (GRAYSPSTM) (see Fig. 2). The second variation is the native pre-modification Gray counter (GRAYPREM) (see Fig. 3). The last variation is Viscor's Gray counter (GRAYIIVN) [5]. GRAYIIVN is a scalable Gray counter with parity generation bit. Besides the GCCD, one other low power architecture that had been examined is the one-hot one-bit shift-register architecture. The following Section is a brief introduction of the one-hot one-bit shift-register architecture.

2.2 One-hot addressing architecture

Isolating and localising switching activities to a small area can reduce the power consumption of an addressing hardware. One-hot addressing architecture is one such hardware architecture that reduces power consumption by isolating switching activities to a small area. The one-hot addressing architecture (OHA) is made up of a chain of one-bit shift-registers as shown in Fig. 4. This architecture consists purely of register-memory logic (i.e. without combinational gates). The number N in the Figure

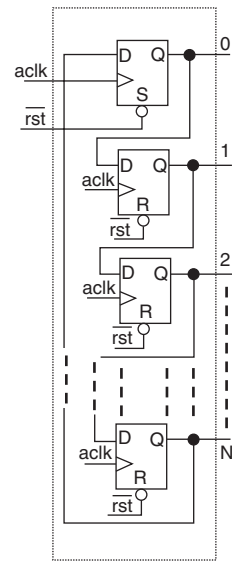


Fig. 4 One-hot shift-register

represents the total number of shift-registers and outputs in the chain.

For this one-bit shift-register OHA to be able to address sequentially, it must first be initialised by setting (or resetting) the first register (at the start of the chain) and resetting (or setting) the remaining registers. Then, by clocking the clock inputs of the registers, the active bit is shifted down the chain. Hence, the active bit, acting like an address pointer (see Table 1), enables the OHA to advance sequentially. The output of each of the registers will serve as an address pointer/selector. As it is 'one-hot', only one register is active at one time. Therefore, this architecture has a constant and low number of switching activity (of 2 transitions per address advance). As a result, it is relatively faster than a CCD architecture.

An architecture similar to the OHA was used by Tsern and Meng [6] as a FIFO address pointer. Unfortunately, it is not low power since its depth size is 16 (which is greater than 4). The proof and reasons why this architecture is not low power will be presented in Section 5. Another variation of the OHA was proposed by Wu and Pedram [7]. The one-hot-zero utilises all-zeros state as a valid state to reduce the total of flip-flops in the chain. Although, the all-zeros state results in a OHA architecture that is inherently clock gated, it still needs extra logic to produce a single select-enable signal line for the all-zeros state.

3 Multi-segments multi-level OHA (MSML-OHA)

The shortcomings of the traditional OHA can be overcome with the proposed multi-segments multi-level one-hot addressing architecture. The multi-segments multi-level OHA (MSML-OHA) consists of many smaller segments of OHA that are designed to break-up the original long single one-hot chain. The structure of each segment of the one-hot chain is the same as the original one-hot chain (see Fig. 4). The architecture is termed as multi-level as its originating clock signal has to propagate through levels of logic gates before reaching its final output. By segregating the OHA's one-hot chain into multi-segments and combining its output by layers of AND gate array clusters, switching activities can be contained effectively in a small area. As this architecture is made up of segments of one-hot chain and clusters of AND gate arrays, it is scalable and has many different possible configurations of multi-segments

Table 1: Output of OHA against number of clock tick

Clock event	Output port select '7'	Output port select '6'	Output port select '5'	Output port select '4'	Output port select '3'	Output port select '2'	Output port select '1'	Output port select '0'
Tclk = 0	0	0	0	0	0	0	0	1
Tclk = 1	0	0	0	0	0	0	1	0
Tclk = 2	0	0	0	0	0	1	0	0
Tclk = 3	0	0	0	0	1	0	0	0
Tclk = 4	0	0	0	1	0	0	0	0
Tclk = 5	0	0	1	0	0	0	0	0
Tclk = 6	0	1	0	0	0	0	0	0
Tclk = 7	1	0	0	0	0	0	0	0
Tclk = 8	0	0	0	0	0	0	0	1
Tclk = 9	0	0	0	0	0	0	1	0
Tclk = 10	0	0	0	0	0	1	0	0
Tclk = 11	0	0	0	0	1	0	0	0
Tclk = 12	0	0	0	1	0	0	0	0
Tclk = 13	0	0	1	0	0	0	0	0
Tclk = 14	0	1	0	0	0	0	0	0
Tclk = 15	1	0	0	0	0	0	0	0

OHA. The following Subsections describe some of the possible configurations that have been explored.

3.1 Double-segment double-level OHA (DSDL-OHA)

As mentioned in Section 2.2 the conventional OHA is not low power (compared to CCD) when the depth size is greater than 4. In order to achieve low power consumption at depth sizes of more than 4, a double-segment double-level (DSDL) OHA is proposed. The DSDL-OHA consists of two segments of one-hot shift-registers that are individually chained as shown in Fig. 5. It is termed 'double-level' because the originating clock signal has to propagate through two levels (or layers) of logic gates before reaching its final output as seen in Fig. 5.

In this case, the originating clock has to be gated first through the one-hot shift-registers and then through the AND gate array. The output of OHA is combined and gated through one level of the AND gate array (see Fig. 6). Each AND gate array consists of two sets of inputs. The two sets of inputs are the main inputs (inN) and the enable input (enb_in). The input data signals destined for the outputs are connected to the main inputs. An active signal (of logic 'high') on the enable input will switch the input signal to the outputs otherwise the outputs will remain inactive (logic 'low'). By dividing the one-hot shift-registers into two segments and combining these with an AND gate array, the number of outputs of the first segment is effectively multiplied by the second segment. For instance, in the DSDL-OHA (seen in Fig. 5) the effective depth size of the addressing architecture is 16 (4×4).

There are two sets of OHAs in the DSDL-OHA 4×4 configuration as shown in Fig. 5. All the outputs of the first OHA are connected directly into the main inputs of all the AND gate arrays. Whereas each of the outputs of the second set of OHAs are connected to the enable input of each AND gate array. When the DSDL-OHA is clocked, the first set of OHAs will advance sequentially. However, the second set of OHAs will only advance if the fourth output of the first OHA (Fsel_3) is active when it is clocked. Therefore, only one AND gate array cluster is enabled

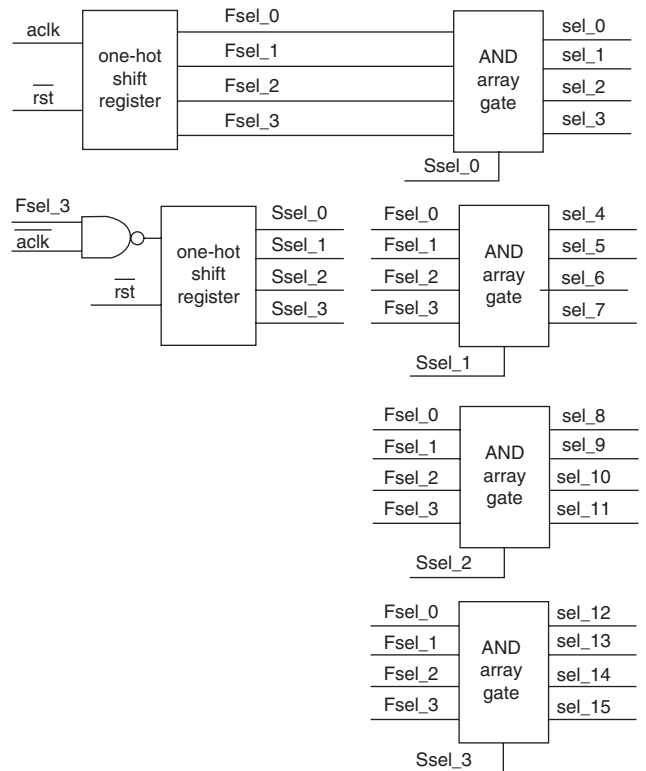


Fig. 5 DSDL-OHA 4×4

every 4th clock cycle. The enabled AND gate array will then gate the output signal of the first OHA through to its output.

As the signal from the registers passed through only one level of AND gate arrays, this architecture is (one combinational gate delay) slower than OHA. However, as a single gate delay is small, it does not have much of an impact on its performance. The propagation delay of the switching is fairly constant except in instances when a signal rollover from segment to segment occurs (i.e. at the moment when the AND gate array is enabled).

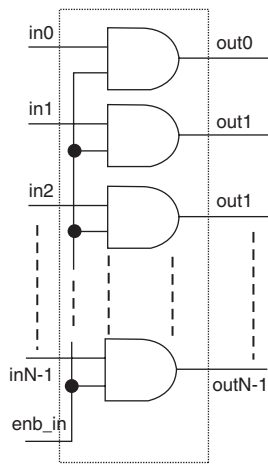


Fig. 6 AND gate array

3.2 Triple-segment double-level OHA (TSDL-OHA)

This concept of segmentation is further extended to get two variations of three segments OHA. One of these is the triple-segment double-level (TSDL) OHA. This TSDL-OHA (Fig. 7) has one OHA segment more than a DSDL-OHA. Instead of a 2-input AND gate array, TSDL-OHA uses a 3-input AND gate array. With this third segment, the number of outputs is multiplied yet again. Like the DSDL-OHA, the TSDL-OHA combines the output of the segments of OHA with one level of AND gate arrays. As such, the nominal delay for TSDL-OHA is one combinational gate delay slower than OHA. However, in cases where there is a signal rollover from one segment to another segment, the worst case propagation delay is two combinational gate delays longer than OHA. This is due to the fact that the signal needs to ripple from the first OHA segment through to the third segment. Hence, the propagation delay is not constant.

3.3 Triple-segment triple-level OHA (TSTL-OHA)

The triple-segment triple-level (TSTL) OHA (Fig. 8) is similar to TSDL-OHA except that it has another level of AND gate array added to it. This architecture is the slowest architecture presented in this paper because of the third level of logic gates the signals have to propagate through. However, the addition of another level of AND gate arrays has a profound impact on its power consumption. The power consumption figure of the TSTL-OHA will be presented in Section 4.2. Like the DSDL-OHA, this architecture uses its second and third segment outputs to individually control signal gating at the first and second AND gate array.

4 Power evaluation results

The power analysis is divided into three main parts. The first part of the power evaluation focuses on OHA. Power comparisons with CCD architecture will be made. The second part of the power evaluation focuses on the DSDL-OHA, TSDL-OHA, TSTL-OHA, CCD and three variations of GCCD circuits. Results of these power evaluations will be compared against the power consumption figures of CCD. The power consumption figures of the three GCCD circuits are presented for reference only. All designs were coded at the register transfer level (RTL) in Verilog

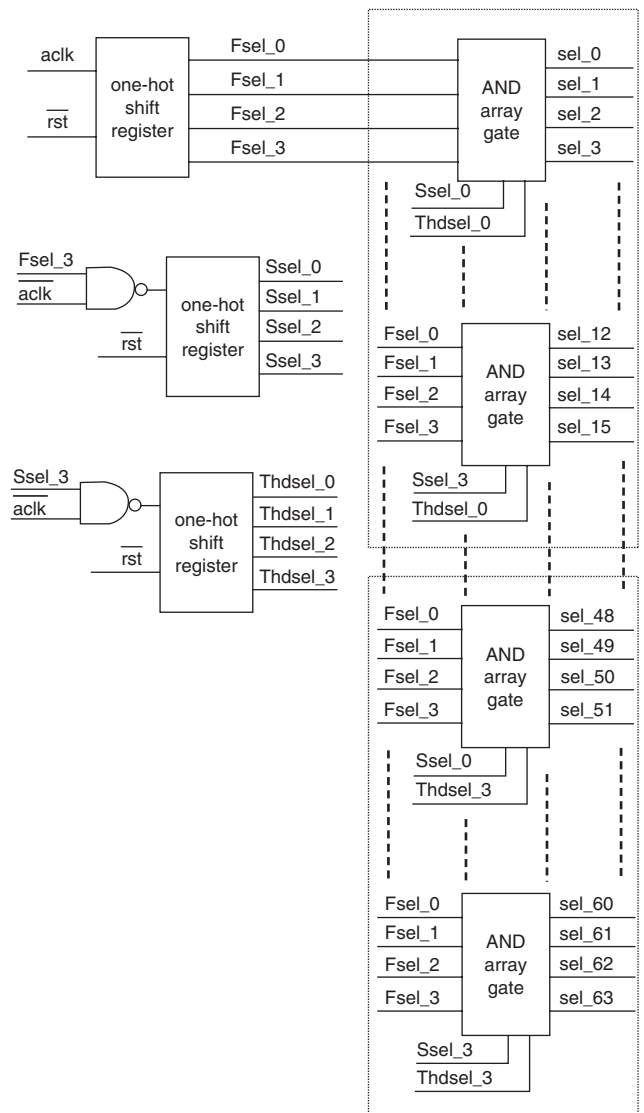


Fig. 7 TSDL-OHA $4 \times 4 \times 4$ architecture

hardware description language (HDL). Cadence's Verilog-XL™ was used to verify and simulate the functionality of the designs. These designs were synthesised to UMC 0.18 μm technology with Synopsys's Design Compiler. Power analyses of these designs were performed using Synopsys's Power Compiler.

4.1 OHA

Results from the power evaluations on the OHA at depth 4, 8 and 16 are as shown in Table 2. The negative values in Table 2 indicates a reduction in power consumption while a positive value indicates an increase in power consumption. It can be seen from Table 2 that there is a significant power reduction with OHA at the depth size of 4. The power saving is due mainly to the absence of the combinational gate decoder. However, at the depth size of 8, the power consumption of OHA had exceeded the power consumption of CCD as the power consumed internally by the shift register flip-flops is slowly dominating the power consumption figures. At a depth of 16, the power consumption of OHA had in fact increased by 52%. This is due to the fact that the power saved by the absence of the combinational gate decoder has been overwhelmed by the amount of power consumed internally by shift register flip-flops.

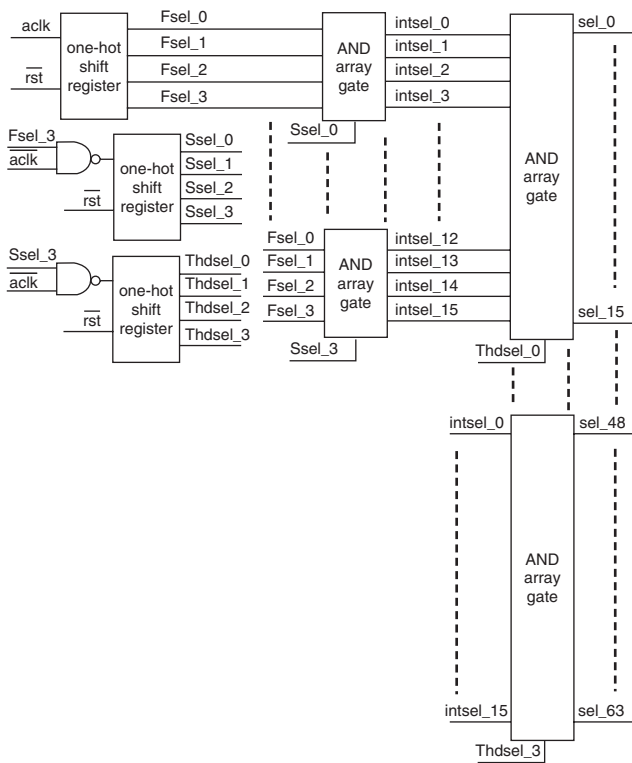


Fig. 8 TSTL-OHA $4 \times 4 \times 4$ architecture

Table 2: Power evaluation results of OHA

Depth size	Type of Architecture	Power (μ W)	Power difference (μ W)	Power difference %
4	CCD	67.24680	-4.5527	-6.77
	OHA	62.69410		
8	CCD	98.55620	5.9256	6.01
	OHA	104.818		
16	CCD	127.7031	66.9773	52.45
	OHA	194.6804		

4.2 Multi-segment multi-level OHA

Power evaluations were performed on the multi-segment OHA with time duration of 1028 clock events. As the meaningful minimum number of register in an OHA is 4, entries for DSDL-OHA commence from a depth size of 8. In the same way, entries for TSDL-OHA and TSTL-OHA commence from a depth size of 16.

4.2.1 Depth size of 8, 16 and 32: Table 3 stipulates the results of the power evaluations on DSDL-OHA at depth sizes of 8, 16 and 32. This Table also shows the results of TSDL-OHA and TSTL-OHA at depth sizes of 16 and 32. As the depth size of the architecture is a product of the number of registers in the first segment and second segment, different combinations of the number of registers can be used to achieve the same depth size. As such, there are two different DSDL-OHA entries each at depth size of 16 and 32. Likewise, there is more than one combination for TSDL-OHA and TSTL-OHA at depth sizes greater than 64. As seen from Table 3, different combinations of register numbers can affect the power consumption of the addressing architecture.

Table 3: Power evaluation results of multi-segment OHA at depth size of 8, 16 and 32

Depth size	Type of Architecture	Power (μ W)	Power difference (μ W)	Power difference %
8	CCD	98.5562	-	-
	DSDL-OHA- 4×2	93.988	-4.5682	-4.64
	GRAYSPSTM	98.2081	-0.3481	-0.35
	GRAYPREM	69.0266	-29.5296	-29.96
	GRAYIIVN	122.0181	23.4619	23.81
	CCD	127.7031	-	-
16	DSDL-OHA- 8×2	134.1386	6.4355	5.04
	DSDL-OHA- 4×4	109.0329	-18.6702	-14.62
	TSDL-OHA- $4 \times 2 \times 2$	113.5968	-14.1063	-11.05
	TSTL-OHA- $4 \times 2 \times 2$	115.6991	-12.004	-9.4
	GRAYSPSTM	133.93	6.2269	4.88
	GRAYPREM	99.5878	-28.1153	-22.02
	GRAYIIVN	154.8411	27.138	21.25
	CCD	149.2158	-	-
32	DSDL-OHA- 8×4	146.3853	-2.8305	-1.9
	DSDL-OHA- 4×8	149.8705	6.547	0.44
	TSDL-OHA- $4 \times 4 \times 2$	143.0786	-6.1372	-4.11
	TSTL-OHA- $4 \times 4 \times 2$	129.3281	-19.8877	-13.33
	GRAYSPSTM	156.6559	7.4401	4.99
	GRAYPREM	121.4398	-27.776	-18.61
	GRAYIIVN	183.2336	34.0178	22.8
	CCD	149.2158	-	-

Results from Table 3 show that there is no significant power reduction shown for both TSDL-OHA and TSTL-OHA at all depth sizes and for DSDL-OHA at a depth of 8. This is because the power saved by the absence of a combinational gate decoder has been overtaken by the additional power consumption needed for gating the signal from the OHA segments to the output. In order for any of the MSML-OHA to be low power, the power saving owing to the absence of the combinational gate decoder must be significantly greater than the additional power consumed by the OHA segments and the additional logic needed for gating the signal from the OHA segments to the output. At depth sizes of 16 and 32, significant power reduction can be observed from DSDL-OHA 4×4 and 8×4 as the combinational gate decoder (in the CCD) starts to consume more power than the DSDL-OHA. Significant power reductions were observed from both TSDL-OHA and TSTL-OHA at depth sizes of 16 and 32. Note that GRAYPREM had a significantly lower power consumption figure than CCD at all depth sizes. The reasons why GRAYPREM has a significantly lower power consumption figure than CCD at most depth sizes will be discussed in Section 5.

4.2.2 Depth size of 64 and 128: Table 4 shows the power evaluation results of DSDL-OHA, TSDL-OHA and TSTL-OHA at depth sizes of 64 and 128. Note that at a depth size of 128, there are three different entries each for TSDL-OHA and TSTL-OHA. From the Table, it can be seen that all the addressing architectures except for DSDL-OHA- 8×8 , TSTL-OHA and GRAYPREM have noticeable increases in power consumption. At a depth size of 64, most of the MSML-OHA power consumption has increased because all the MSML-OHA (except for

Table 4: Power evaluation results of multi-segment OHA at depth size of 64 and 128

Depth size	Type of Architecture	Power (μ W)	Power difference (μ W)	Power difference %
64	CCD	186.4241	-	-
	DSDL-OHA- 16×4	267.5913	81.1672	43.54
	DSDL-OHA- 8×8	179.6066	-6.8175	-3.66
	DSDL-OHA- 4×16	268.1107	75.6866	40.60
	TSDL-OHA- $4 \times 4 \times 4$	218.2394	31.8153	17.07
	TSTL-OHA- $4 \times 4 \times 4$	139.7555	-46.6686	-25.03
	GRAYSPSTM	194.7341	8.31	4.46
	GRAYPREM	161.8555	-24.5686	-13.18
	GRAYIIVN	205.9668	19.5427	10.48
	128	CCD	218.4988	-
DSDL-OHA- 16×8		296.6027	78.1039	35.75
DSDL-OHA- 8×16		271.6477	53.1489	24.32
DSDL-OHA- 4×32		477.034	258.5352	118.32
TSDL-OHA- $4 \times 4 \times 8$		345.6864	127.1876	58.21
TSDL-OHA- $8 \times 4 \times 4$		249.6914	311.926	14.28
TSDL-OHA- $4 \times 8 \times 4$		350.6171	132.1183	60.47
TSTL-OHA- $4 \times 4 \times 8$		169.072	-49.4268	-22.62
TSTL-OHA- $8 \times 4 \times 4$		173.8137	-44.6851	-20.45
TSTL-OHA- $4 \times 8 \times 4$		184.5725	-33.9263	-15.53
GRAYSPSTM		213.338	-5.1608	-2.36
GRAYPREM		173.9401	-44.5587	-20.39
GRAYIIVN		245.0896	26.5908	12.17

TSDL-OHA) had more than 4 shift-register flip-flops in one of its OHA segments. However, TSTL-OHA is able to gain a significant amount of power reduction, as switching activities within its architecture are restricted to only a small area and the switched capacitances were kept low with the 3 levels configuration. At a depth size of 64, the TSDL-OHA- $4 \times 4 \times 4$ power consumption has increased even though none of its OHAs is greater than 4. This is the result of a significant increase in switched capacitance caused by the substantial increase in the number of connections from the OHA segments to the AND gate array inputs. Note that the power consumption figures of GRAYPREM at all depth sizes remain significantly lower than CCD.

4.2.3 Depth size of 256: The results of the DSDL-OHA power consumption were not included in Table 5 as their values were too high. However, three more entries were added for both TSDL-OHA and TSTL-OHA. These bring the number of configuration entries to a total of 6 for each of the two types of architecture. From the results, all but GRAYPREM and the three TSTL-OHA entries had an increase in power. TSTL-OHA- $4 \times 8 \times 8$, $8 \times 4 \times 8$ and $8 \times 8 \times 4$ were the three that possess a low power characteristic. These TSTL-OHAs were able to have significantly lower power consumption figures compared to CCD because these TSTL-OHAs keep switching activities to small designated areas and keep the switched capacitance low with the 3 levels configuration. This saved power was significant enough to overwhelm the power dissipated by the combinational gate decoder and the 8 bit counter in the CCD. The rest of the architectures showed in Table 5 recorded a huge increase in power consumption. This is because the power consumed by the large number of

Table 5: Power evaluation results of multi-segment OHA at depth size of 256

Depth size	Type of Architecture	Power (μ W)	Power difference (μ W)	Power difference %
256	CCD	227.4345	-	-
	TSDL-OHA- $4 \times 8 \times 8$	694.4802	467.0457	205.35
	TSDL-OHA- $8 \times 4 \times 8$	392.2524	164.8179	72.47
	TSDL-OHA- $8 \times 8 \times 4$	395.3532	167.9187	73.83
	TSDL-OHA- $4 \times 4 \times 16$	702.5144	475.0799	208.89
	TSDL-OHA- $4 \times 16 \times 4$	727.9153	500.4808	220.05
	TSDL-OHA- $16 \times 4 \times 4$	367.8219	140.3874	61.73
	TSTL-OHA- $4 \times 8 \times 8$	205.8099	-21.6246	-9.51
	TSTL-OHA- $8 \times 4 \times 8$	201.5815	-25.853	-11.37
	TSTL-OHA- $8 \times 8 \times 4$	205.7926	-21.6419	-9.52
	TSTL-OHA- $4 \times 4 \times 16$	270.2504	42.8159	18.83
	TSTL-OHA- $4 \times 16 \times 4$	296.5934	69.1589	30.41
	TSTL-OHA- $16 \times 4 \times 4$	294.0331	66.5986	29.28
	GRAYSPSTM	246.1017	18.6672	8.21
GRAYPREM	199.1029	-28.3316	-12.46	
GRAYIIVN	270.3817	42.9472	18.88	

shift-register flip-flops and the additional gating logic in the MSML-OHA exceeded that of the CCD.

5 Discussion

Figure 9 shows the best case power savings of OHA, MSML-OHA architectures and three variations of GCCD at different depth sizes. A positive value in the Figure represents the percentage of power saving compared to a CCD architecture. A negative value indicates that the addressing architecture is consuming more power than CCD architecture. From the results presented in the above Section and Fig. 9, it can be seen that there is a significant power reduction at depth size of 4 for OHA. The Figure also shows that the multi-segment OHAs have significant power reduction at all depth sizes (except at 4). It can also be seen that only one type of the multi-segment OHA architectures is power efficient at a certain range of depth sizes. OHA is power efficient at a depth size of 4. DSDL-OHA is power efficient at a depth size of 8 to 64. TSTL-OHA is power efficient from a depth size of 16, all the way to a depth size of 256. Finally TSDL-OHA is power efficient at a depth size of 16 and 32. It can be seen from Fig. 9 that overall the multi-segment OHA reduces on average about 20% of the power compared to CCD.

From Section 4.2, it is apparent that not all the MSML-OHAs are low power compared to the CCD. Whether or not a MSML-OHA is low power, depends greatly on combinational gate switching activities and the number of clocked registers in the architecture. In Section 2.1, it was mentioned that a considerable amount of power is consumed when the switching signal ripples through layers of the combinational gates in the addressing architecture. However, these combinational logic components are not the sole contributors to the increased power. The total number

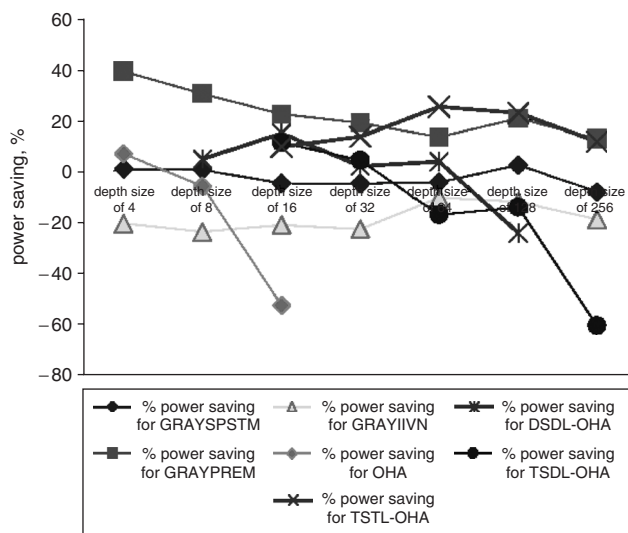


Fig. 9 Best case power saving (wrt CCD) at different depth sizes

of flip-flop registers in the whole address, the number of flip-flop registers in each segment and the sequence of how the segments are arranged affects greatly the of the power consumption addressing hardware. The amount of power that the segment sequence can bear can be seen in the DSDL-OHA at a depth size of 32 when the sequence of the number of flip-flops is changed from 8×4 to 4×8 . All of these is due to the fact that the edge-triggered flip-flop consumes about 3 times more power than a combinational gate when it is clocked, even without any state change at the output (see Table 6). The power consumption values in Table 6 were obtained from power evaluating a D-type flip-flop and a 2 input AND gate over 300 clock events at clock period of 10ns. The above-mentioned attribute is also the reason why OHAs are not low power (see Section 4.1) when the depth size is greater than 4. The power saving achieved by eliminating the combinational gate switched capacitance is soon overtaken by the internal power consumption of clocked flip-flops. As such, by reducing the total number of registers in the addressing architecture and the number of registers in a single one-hot chain where frequent switching takes place, the overall power consumption will be reduced. Therefore, by segregating the OHA's one-hot chain into multi-segments and combining the outputs with a group of AND gate arrays to form MSML-OHA, the power consumption in the register-memory logic is minimised. However, by combining its outputs with a group of AND gate arrays creates extra combinational logic switching capacitance. Therefore, in order to achieve power reduction, an optimal combination of the number of segments and registers in the addressing architecture need to be determined. The optimal combination can be obtained by an

Table 6: Power consumption of AND gate compared with D-type flip-flop (power consumption values were obtained from 300 clock cycles of power evaluation)

	Power (μ W)	Power difference (μ W)	Power difference %
D-type flip-flop	6.970100	-	-
AND gate	1.940772	-5.029328	-72.16

empirical method which is the approach adopted in this research.

From Fig. 9 and the power evaluation results shown in Section 4.2, it is noticeable that all GCCD (except for GRAYPREM) consumed more power than CCD. It is not surprising that the power consumption of GRAYSPSTM is almost identical to those of CCD as GRAYSPSTM is simply a binary counter attached with a combinational gate (XOR) binary to a Gray code converter. Glitches in the binary-to-Gray-code converter logic owing to the settling of multi-bits (binary number) switching caused the power consumption of GRAYSPSTM to rise by a small amount. Although GRAYIIVN is a native Gray counter, it consistently consumes more power than CCD. This is because it has one extra flip-flop register and combination gate in its design. In addition, internal glitches caused by propagation of the parity-bit-derived signal for the computation of the next Gray code value, further increase the power consumption of the GRAYIIVN (see [5] for details of its design). GRAYPREM's power consumption is consistently lower than that of CCD because it is a native Gray counter that outputs clean Gray code without glitches. Although GRAYPREM seems to be a good alternative as a low power counter-decoder, there is no concise, regular, scalable and portable way of coding its design at present. Hence, GRAYPREM had to be hard coded for each desired depth size. The MSML-OHAs, however, are scalable with regular structures. They can also be scaled up to higher segments and levels. However, by scaling up, signal propagation delay will also increase as the level and number of segment increases. This increase in signal delay nevertheless will be fairly constant, except when a signal rollover from segment to segment occurs.

The MSML-OHA occupies a larger area of about 25% to 45% than CCD with the majority of this increase in area caused by the OHA registers segments. The OHA registers segments occupy about 45% to 73% of the total area for DSDL-OHA, 27% to 65% for TSDL-OHA and 22% to 58% for TSTL-OHA. The area occupied by the OHA registers segments (with respect to the total area) in the MSML-OHA decreases as the depth size increases.

6 Conclusion

In this paper, multi-segments multi-level one-hot addressing architectures (MSML-OHA) were presented. MSML-OHA are made up of individual chains of one-hot shift registers segments and clusters of combinational AND gate arrays. The MSML-OHA is suitable for applications that require large amounts of all-sequential addressing like FIFOs and round buffers addressing hardware use in (hardware) digital filtering and image signal processing. The MSML-OHA is the outcome of optimisation done at the architecture level by containing and isolating switching activities to a small confined local area. Power evaluation results show that MSML-OHAs reduced an average of more than 20% power compared to conventional counter-decoder addressing architecture (CCD). Hence, isolating switching activities into a small local area by segmenting the overall architecture into a smaller area is effective in reducing switching activity area and thus the power consumption of the architecture. It is concluded that local architectural level optimisation can reduce the power consumption of sequential addressing hardware significantly. The multi-segment OHA is scalable and can be optimised by using different combinations of register numbers. Such architectures are suitable to be used as part of any low power system to trade off area and speed for reduction in power consumption.

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