A LOW POWER COMBINER CIRCUIT FOR MULTI-CARRIER CDMA

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The power consumption of multi-carrier CDMA receivers implemented in digital hardware is considered. A low power block based architecture is investigated for the combiner sub-system, and compared with a multiply accumulate circuit approach. Simulations using data consistent with typical performance of a multi-carrier CDMA receiver indicate that the block based approach can produce a power reduction of around 50%.

1 INTRODUCTION

Multi-Carrier CDMA (code division multiple access) [1, 2] is a spread spectrum technology which combines the advantages of OFDM (orthogonal frequency division multiplexing) and CDMA to produce a spectrally efficient multi-user radio access system which may be applied in future mobile wireless systems beyond the 3rd generation. In such systems, the power consumption of a mobile receiver may be a significant issue. A multi-carrier CDMA receiver contains two main system blocks, an FFT block to demodulate the OFDM signals and a combiner block which equalises the signal and separates out the coded users. The combiner can employ a variety of techniques such as simple RAKE filtering (MRC - maximal ratio combining), or decorrelating or even minimum mean square error multi-user detection to isolate the users signal. The minimisation of power consumption of the FFT has been the subject of numerous papers [3, 4, 5, 6], and many of these techniques could be applied in a multi-carrier CDMA receiver. Therefore in this paper only the minimisation of the power consumed in the combiner block is considered.

2 MULTI-CARRIER CDMA

The multi-carrier CDMA considered in this paper uses one code chip per carrier and should not be confused with direct sequence CDMA systems transmitted on multiple carriers [7]. The signal is spread before being converted into a parallel data stream which is then transmitted over multiple carriers. If the processing gain is equal to the number of carriers then this system modulates all the carriers with the same data bit, but with a phase shift on each carrier determined by the spreading code. This is shown in figure 1. This multi-carrier modulation can also be implemented using an inverse FFT.

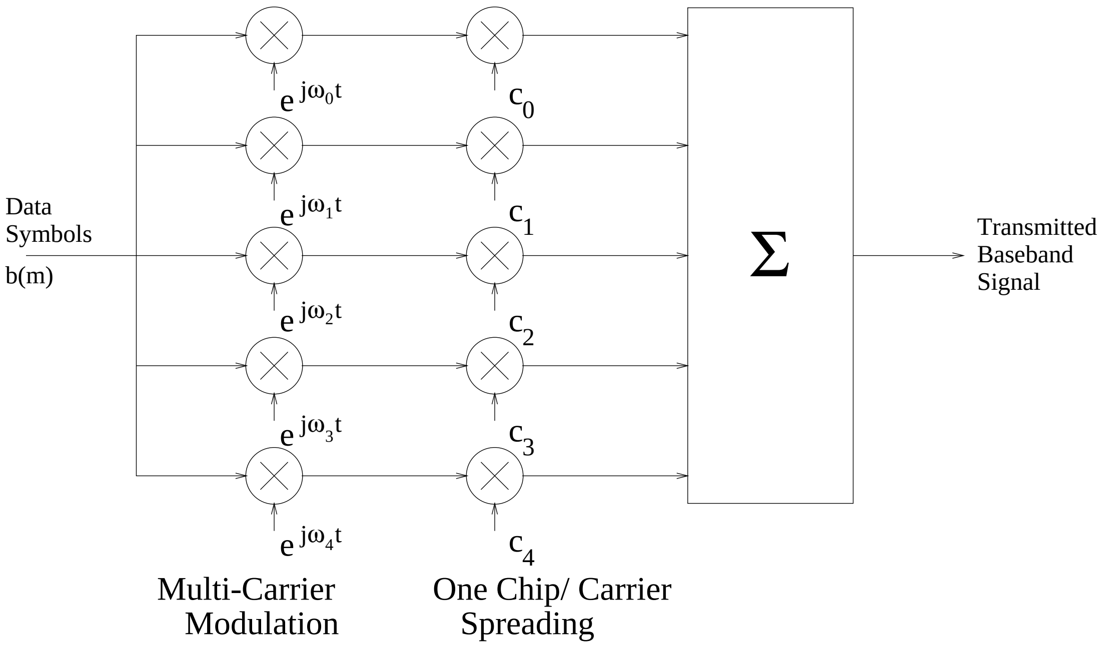

Figure 1: Multi-carrier CDMA transmitter

If the kth chip of the spreading code for user u is defined as $c(k, u) \in \{-1, +1\}$ then the transmitted baseband signal for mth data symbol $b(m)$ is:

$$x(n) = \sum_{n=0}^{N-1} \exp(j2\pi kn/N)c(k, u)b(m) \tag{1}$$

To overcome the effect of inter-symbol interference, this baseband signal is cyclically extended by more than the channel delay spread, to allow transmission of an interference free symbol. By using a guard interval, the receiver selects the portion of the signal that is free from inter-symbol interference. This is processed by an FFT block to demodulate the multiple carriers.

The effect of a multipath channel $h(n)$ at the output of the FFT is narrowband for each carrier, $H(k)$, and therefore the equalisation and despreading can be incorporated into a single combining operation to estimate the transmitted data bit. If the output of the FFT block at frequency bin k is defined as $Y(k)$ then the combining operation can

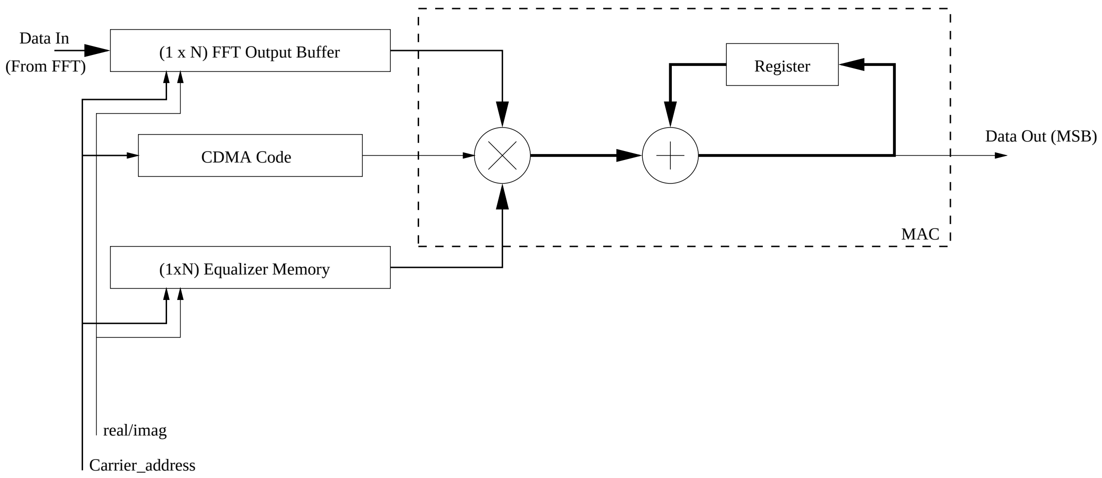

Figure 2: Combiner incorporating Multiply Accumulate Circuit

be represented by:

$$\hat{x}(n) = \text{sign}\{\sum_{k=0}^{N-1} \Re\{c(k,u)A(k)Y(k)\}\} \tag{2}$$

The equaliser coefficient $A(k)$ can be used to implement a frequency domain rake filter if it is set to match the channel: $A(k) = H^*(k)$. Linear multi-user detection can also be implemented by simply changing the coefficient $A(k)$. A decorrelator can be implemented by setting $A(k) = H^*(k)/|H(k)|^2$ and the MMSE (minimum mean square error) solution can be implemented using $A(k) = H^*(k)/(|H(k)|^2 + \lambda)$ where λ is a parameter dependent upon the signal to noise level and the number of users.

The implementation of this combiner can be achieved using a multiply accumulate unit as shown in figure 2 for an N carrier system. In this architecture, the output of the FFT and the equaliser coefficients ($A(k)$) are buffered and a serial multiply accumulate performed to obtain the data bit estimate. Since the code chips can only be +1 or -1, the multiplication by these chips is achieved by changing the sign of the product as required.

3 A LOW POWER MC-CDMA ARCHITECTURE

The power consumption of a circuit can be cut by reducing the amount of switching. In the MAC based architecture, both inputs to the multiplier are switched every clock cycle as new input data samples and equaliser coefficients are multiplied. Since the multiplier is the largest component in the circuit, reducing the amount of switching here should have a large effect on the power consumption.

A block based approach [8] has previously provided an effective method for producing a low power DCT. In the case of a MC-CDMA receiver, a similar approach can be applied, if it is assumed that the channel fading is sufficiently slow that it allows the use of the same channel equalisation coefficient for a significant block length.

Under these conditions, a block of data containing M symbols can be buffered. The data is then processed, one carrier at a time for the entire block length of symbols. A block of memory is used to store the accumulated total for each symbol, and the MSB of each word provides the data estimate for each symbol. Figure 3 shows the architecture for this circuit.

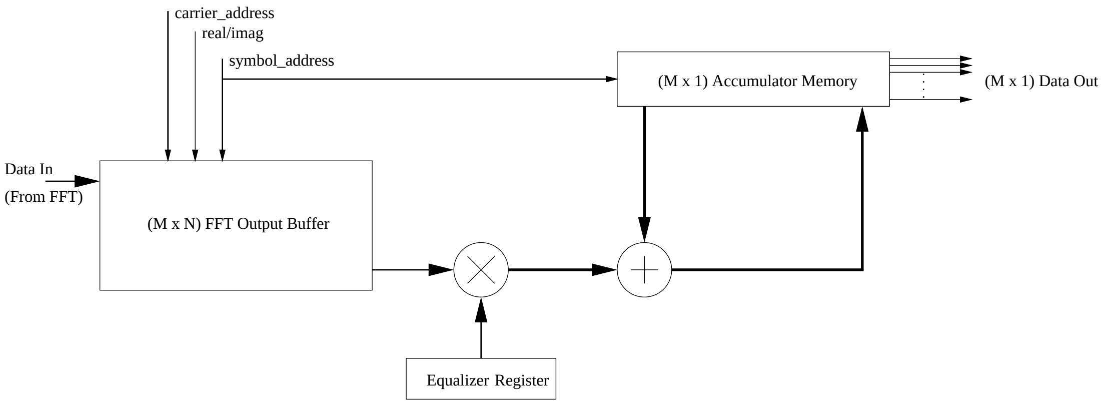

Figure 3: Low Power Block Based Combiner

The detailed operation of this architecture proceeds as follows. The first symbol of the first carrier is processed. This first symbol is a pilot used for channel estimation, and both the real and imaginary values of the received symbol are used to set the appropriate coefficient value. The sign of this coefficient is also dependent on the CDMA code chip for the first carrier. The remainder of the real parts of the symbols from the first carrier are then multiplied by the real part of the equaliser coefficient, and stored in separate addresses in the accumulator memory. The imaginary parts of the first carrier are then also processed, multiplying by the imaginary part of the equaliser and then being subtracted from the acummulator memory values to produce the desired real component of the complex multiplication. The algorithm then moves onto the second carrier. This is processed in the same way as the first except that the real products are added to the appropriate address in the accumulator memory. The remaining carriers are processed in the same way, a block at a time, until all the carriers have been processed. At this point, the most significant bit in each of the accumulator memory elements indicates each transmitted symbol value.

Architecture	Cell Area	Power (1 User)	Power (16 Users)
MAC	28166.56	26.7923 mW	25.9522 mW
Block	14415.76	12.9790 mW	13.9464 mW

Table 1: Comparison of MAC Based and Block Based Architectures

The principal result of this architecture is that the equaliser coefficient and the CDMA code are held constant for M clock cycles, therefore one input to the multiplier is switched at a much lower frequency and hence the resulting power consumption should be significantly lower.

4 POWER ANALYSIS

To evaluate the power consumption of the proposed architecture, both the MAC based combiner and the low power block based combiner were synthesised using Ambit Buildgates and the Alcatel 0.35μ library. Power analysis was performed on the synthesised model using Synopsis Design Power assuming a clock rate of 10 MHz and data symbol rate of 156 kHz. This analysis was restricted to measuring the dynamic power consumption due to switching.

A 64 carrier system was assumed and the data were divided into blocks of 32 symbols, with the first symbol in the block being used as a pilot for channel estimation. A word length of 16 bits was assumed for the output data from the FFT block. Additional circuitry was included to estimate the channel coefficients, including a division circuit, however the multiply unit can be reused. These do not increase the power consumption significantly as they are only used for 1 out of 32 symbols.

Simulations were performed using a single user scenario and a scenario with an additional 15 interfering users modelling typical performance of the system.

Random CDMA codes were generated for the pilot symbols and for one user. The data for the single user scenario were generated by spreading known pilot symbols and random binary data symbols by CDMA codes. The spread symbols were multiplied by complex Gaussian random variables to model the effect of passing through parallel Rayleigh fading narrowband channels, and giving the appropriate value for the FFT output at the receiver. No explicit Gaussian additive noise was added, and the noise variance parameter in the MMSE equaliser, λ, was set arbitrarily to the value of 1. For the scenario with 15 interfering users, Gaussian distributed noise was added to the signal at the power level of 15 interfering users.

The cell area and switched power consumption for both circuits are shown in table 1. It is clear that the block architecture significantly reduces the power consumed in both cases to a level that is approximately half that of the MAC based architecture, which is to be expected as only one input of the multiplier is switched at a high frequency. The block based architecture also reduces the size of the circuit, although this is due to the block size and number of carriers: the 128x16 bit words of memory required for 64 complex equaliser coefficients are replaced by 32x32 bit words for accumulating the products. This does not take into account the larger buffer for storing FFT outputs which would be required and this would actually make the block based architecture significantly larger. However since this memory is accessed no faster than the smaller memory of MAC architecture, then the switched power consumption will not significantly increase.

5 CONCLUSIONS

In this paper a low power architecture for multi-carrier CDMA systems has been investigated. This architecture can be used to implement a frequency domain rake receiver or a multi-user detector such as a decorrelator or MMSE receiver. The architecture reduces the power consumption by processing a block of data bits at a time. This allows the equaliser input of the multiplier to remain constant for a large number of clock cycles, reducing the switching in the multiplier and therefore reducing the overall power consumption to half that of a multiply accumulate based system.

6 ACKNOWLEDGEMENT

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