

Implementation of an SIC based MC-CDMA Base Station Receiver

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1 Introduction

Investigation of the performance of uplink multi-carrier code-division multiple access (MC-CDMA) receiver designs [1] has indicated that the inclusion of decision statistic ordered successive interference cancellation (SIC) [2] in the receiver provides good performance for a large number of users with an algorithm of only N^2 complexity. Accurate channel estimation can be a problem in uplink MC-CDMA, but if the channels have a small delay spread, narrowband pilots and interpolation can be applied to provide accurate channel estimates, without requiring a high pilot signal to noise ratio.

The hardware implementation of low power MC-CDMA mobile stations has been considered in [3]. This work is extended to the uplink in this paper. In particular the implementation of the decision statistic ordered SIC algorithm is considered. Although much of the SIC algorithm requires serial operation, some parallelisation can be applied to reduce the number of clock cycles required from N^2 to N . A 48 user QPSK system is considered and therefore a reduction of clock rate from 9216 times the symbol rate to 96 times the symbol rate is desirable, however both serial and parallel architectures will be investigated.

2 Comparison of SIC and ML uplink MC-CDMA

The performance of decision statistic ordered SIC compares favourably with many other multi-user detection algorithms, although it cannot match the performance of the maximum likelihood (ML) joint detection algorithm. Under certain circumstances however the difference between their performance is small. Figure 1 shows the performance of ML and SIC algorithms for uplink MC-CDMA. In this case a system with processing gain of 8 is simulated to keep the simulation time short. Random codes were used and up to 16 simultaneous users were simulated. The graph shows the signal power required to obtain bit error probabilities of 10^{-2} and 10^{-3} .

Clearly up to 7 users, the performance of the algorithms is almost identical however when the number of codes is larger than the processing gain, the performance of SIC deteriorates rapidly. Therefore the algorithm is a very good candidate for systems where the maximum spectral efficiency required is at most 1, and the quality of service requirement is for uncoded probability of error of around 10^{-2} to 10^{-3} .

3 Interpolated Channel Estimation

Transmitting wideband pilot symbols produces several problems in uplink MC-CDMA. Firstly, since multi-user interference will degrade the channel estimation severely, each user needs to be allocated an individual time slot, heavily impacting spectral efficiency. Secondly, since each user transmits an individual pilot (compared to a single joint pilot for the downlink) the available signal power will be much lower.

A more effective method of channel estimation can be easily achieved if the delay spread of the channel is short and hence there is a strong correlation between channel coefficients in neighbouring channels. In these cases, pilots can be transmitted on a few carriers and the rest of the channel estimated by linear interpolation. A large number of users can be supported, transmitting their pilot symbols on different carriers. A time slot for all users to transmit pilot symbols can be allocated of several symbol lengths and each user can transmit several single carrier pilot symbols on different frequencies providing sufficient information to estimate the channel. Figure 2 shows the structure of pilots transmitted in a 16 user/16 carrier system with the time and frequency positions of the pilots of users 2 and 9 indicated.

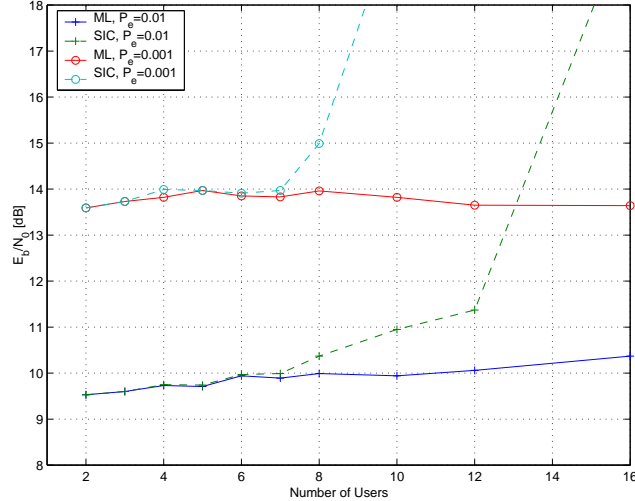


Figure 1: Comparison of ML and SIC algorithm performance for an 8 chip MC-CDMA uplink system in Rayleigh fading channels

Simulations of an uplink MC-CDMA system using this channel estimation method were performed. The specification of the system chosen is a 64 carrier system based on a 20 MHz sampling rate with symbol lengths of 80 samples including a 16 sample cyclic-prefix to compensate for the multipath and asynchronism. This produces a 250kHz symbol rate. The data were divided into blocks of 40 symbols, of which 8 are pilots. Only 48 of the 64 carriers are used to carry data in a similar way to the IEEE 802.11 and HIPERLAN/2 OFDM Wireless LAN standards [4, 5]. With QPSK modulation on the data symbols this produces a system which will have a spectral efficiency of 1 bits/s/Hz with 40 active users, and a 48 user spectral efficiency of 1.2 bits/s/Hz. Figure 3 shows the bit error performance for SIC and channel matched filter (MF) receivers, in 3 tap Rayleigh fading channels.

4 Serial Architecture Implementation of SIC

In a quasi-synchronous uplink MC-CDMA system, the receiver output after channel matched filtering for user k can be given as:

$$y(k)_0 = \mathbf{R}(k, k)x(k) + \sum_{i \neq k} \mathbf{R}(i, k)x(i) + \eta(k) \quad (1)$$

$x(i)$ represents user i 's data bit, \mathbf{R} represents the cross-correlation matrix between the users and $\eta(k)$ the additive Gaussian noise after channel matched filtering.

In the decision statistic ordered SIC algorithm, the user with the largest (in magnitude) value for $y(k)_0$ is decoded first, and then the interference caused by this user is subtracted from all other users. This process is repeated until the data from all users are decoded. Figure 4 shows an architecture for this based on a single cancellation (addi-

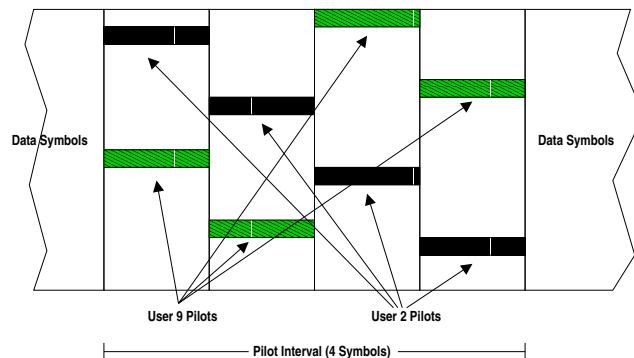


Figure 2: Structure of Pilot Symbol Time Slot for Uplink MC-CDMA

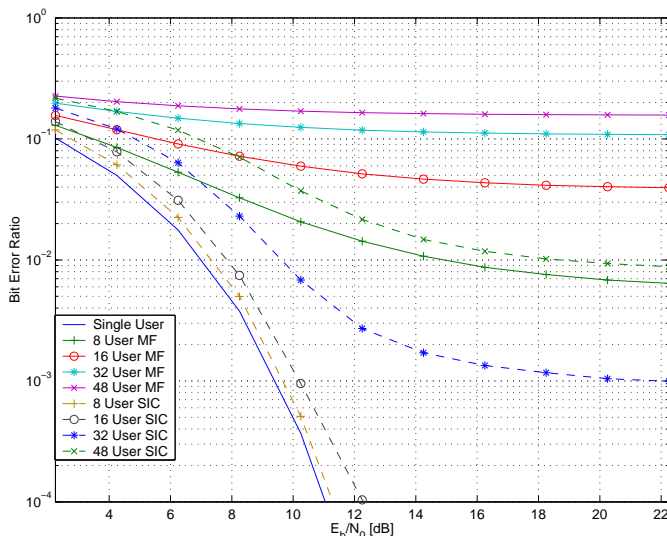


Figure 3: Performance of Uplink MC-CDMA System in Rayleigh Fading Channels

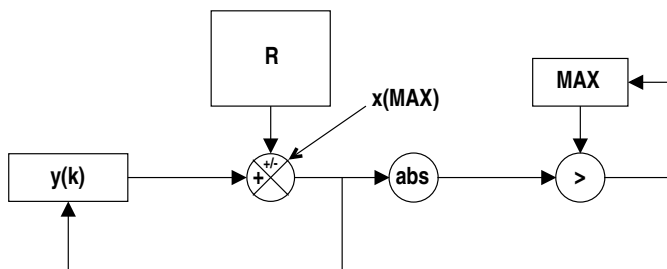


Figure 4: Serial Architecture for SIC

tion/subtraction) circuit, which is switched by the sign of the data value being cancelled. The circuit also computes the absolute value of the new decision statistic and compares this with the existing maximum value at that stage. During the initial cycle, no cancellation are made, but comparisons are made to determine which user's decision statistic has the maximum absolute value. In the subsequent cycles, the operation:

$$y(k)_{t+1} = y(k)_t - R(max, k)x(max) \quad (2)$$

is performed, and the new maximum decision statistic is computed.

To fully compute all user's data symbols requires N^2 clock cycles. If a QPSK 48 user system is considered this requires more than 9000 cycles per symbol. A symbol rate of 2.5×10^5 symbols/s would require a clock rate of over 2GHz. The circuit was synthesised using Verilog and .35 μ CMOS library. Using this technology a clock rate of less than 100 MHz was achievable. Assuming a symbol rate of 2.5×10^5 symbols/s, 20 BPSK or 10 QPSK users could be supported. Obviously a higher clock rate can be obtained by moving to a higher power technology, but the parallelisation of the algorithm also needs to be considered.

5 Parallel Architecture Implementation of SIC

Figure 5 shows a potential parallel architecture for SIC implementation for 4 users. This is not parallel interference cancellation as only one user is cancelled at a time, however the cancellation is applied to all undetected users simultaneously, and the comparisons made to determine the largest magnitude decision statistic are all performed within one clock cycle. This reduces the time to process the symbols to N cycles ($2N$ for QPSK). Therefore to support 48 QPSK users at 2.5×10^5 symbols/s (0.5Mbit/s) would only require a clock rate of 24 MHz which should be easily achievable in low power CMOS hardware.

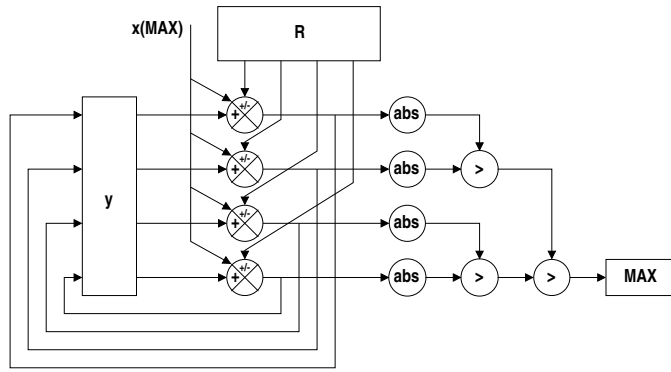


Figure 5: Parallel Architecture for SIC

6 Further Work

The full paper will explore the implementation of the parallel architecture SIC circuit. Details of circuit size, power consumption simulations and achievable clock speeds will be reported. The implementation of the FFT demodulation, channel estimation and channel matched filters will also be investigated. The receiver will also be simulated using the Verilog code to measure the impact on bit error performance of short word length fixed point arithmetic.

References

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