

# ARCHITECTURE AND DESIGN METHODOLOGY FOR SYNTHESIZABLE RECONFIGURABLE ARRAY TARGETING WIRELESS SYSTEM-ON-CHIP APPLICATIONS

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## ABSTRACT

This paper presents a novel domain specific reconfigurable architecture and an associated design methodology for System-on-Chip (SoC) platform which provides flexibility as well as low-power consumption. Two Viterbi decoders, which are widely used in wireless communication systems, are implemented on the proposed architecture using the proposed design methodology. The measured performance shows that our architecture is a perfect compromise between the ASICs and generic FPGAs, and hence suitable for future portable mobile devices.

## I. INTRODUCTION

Future mobile communication systems will not only offer the current services with improved quality, but also new services. Initially, the design for future mobile handsets should be compatible with the old standards. In addition, mobile devices have to provide low power consumption and high throughput in order to be usable for multiple operations. Finally, the time-to-market and low cost requirements have to be fulfilled to strengthen competition. The Reconfigurable System-on-Chip (RSoC) platform <sup>[1] [2]</sup> is emerged to satisfy these entire requirements.

The proposed reconfigurable SoC platform is based on several synthesizable domain specific coarse-grain arrays where each of them is optimized for a specific task. This platform offers an efficient solution for the problems, where a combination of flexibility, low power consumption and high throughput is desirable. In addition, the authors propose the software design flow for generating, programming and verifying the reconfigurable array. Following this design flow, the

designers can easily target any applications on the proposed array architecture automatically.

The paper is organized as follows: Section 2 describes the heterogeneous coarse-grain array architecture. The software design flow for the array architecture is addressed in section 3. Two Viterbi decoders are implemented on the array architecture with the proposed design flow presented in Section 4. The conclusion is assessed in Sections 5.

## II. HETEROGENEOUS COARSE-GRAINED ARRAY ARCHITECTURE

### A. Processing Unit

Each processing unit inside the array architecture is composed of two parts, processing core and I/O interface. The processing core realizes the operation selected by the designer. The interface block routes the input and output signals of the processing unit to four directions. Each direction is connected to the 2-D mesh by the C-boxes. Figure 1 shows the architecture of the processing unit with 2 inputs and 2 outputs. The directions are switched by the multiplexers for the input pins and tri-buffers for the output pins. The routing software can select one of the four directions for each pin depending on the power and timing constraint of the whole system.

### B. C-boxes and S-boxes

The 2-D interconnection mesh, composed of connection-boxes and switch-boxes which are made by multiplexers and tri-state buffers is provided in our array architecture. The connection-boxes allow connecting the input and output pins of the processing unit to the channels. The switch-boxes will connect the metal tracks together.

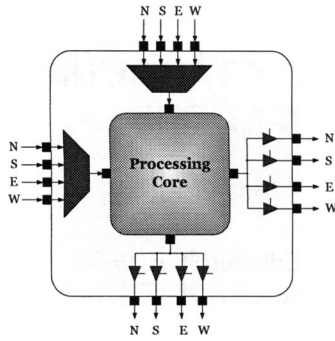


Figure 1 Processing Unit

similar to the output pins of C-boxes, S-boxes use the tri-buffers to switch the connection.

### III. SOFTWARE DESIGN FLOW

Due to the lack of Electronic Design Automatic (EDA) tools for the heterogeneous array architecture, we design our own software to automatically implement specific sets of applications on our array architecture and achieve high performance. The design flow is divided into three stages: array generation, array programming and array verification.

#### A. Array generation

The proposed design flow allows generating arrays for multiple target domains. The resulting array is generated as synthesizable RTL level description.

#### B. Array programming

The array programming stage, the hardware compiler will compile the high level Verilog description into a processing units based netlist file. The place and route tool will automatically place and route the processing units inside array based on timing optimization or power optimization. After generating the routed design, the configuration bits-stream will be generated to configure the array to a specific application.

#### C. Array verification

The verification and performance estimation are done by using the existing ASIC tools, unlike the embedded FPGA architecture where new tools need to be used. Another advantage of using synthesis reconfigurable arrays is that the verification process can include the whole integrated SoC for accurate simulation.

### IV. RECONFIGURABLE ARRAY ARCHITECTURE FOR VITERBI DECODER

Following our software design flow, the RTL level array architecture is generated and programmed to two Viterbi decoders<sup>[3]</sup>, the first one with the constraint length 5, code rate 1/2 and another with constraint length 7, code rate 1/2. And then, both cores are synthesized under 0.18 $\mu$ m technology and estimated the power and area consumption.

The Viterbi decoders are also implemented on the standard 0.18 $\mu$ m ASIC technology and Xilinx Virtex-II FPGA to estimate the trade-off for our array architecture. Comparison results of these two targets on the different architectures are detailed in Table 1 and 2, respectively.

Table 1 Performance of the constrain length 5, code rate 1/2 Viterbi decoder

	0.18 $\mu$ m ASIC	Array Architecture	Xilinx Virtex II
Area (mm <sup>2</sup> )	0.25	1.37	29.16
Power (mW)	2.49	10.37	41.38

Table 2 Performance of the constrain length 7, code rate 1/2 Viterbi decoder

	0.18 $\mu$ m ASIC	Array Architecture	Xilinx Virtex II
Area (mm <sup>2</sup> )	1.54	5.72	207.48
Power (mW)	8.36	50.6	203.32

### V. CONCLUSION

We have presented a novel reconfigurable architecture and an associated design methodology based on a synthesizable heterogeneous coarse-grained array. The array fabric has demonstrated high flexibility as well as good area and power performance, satisfying the requirement for future portable devices.

### REFERENCES

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