

Area & Power Efficient VLSI Architecture for Computing Pseudo Inverse of Channel Matrix in a MIMO Wireless System

Zahid Khan, Tughrul Arslan, John S. Thompson, Ahmet T. Erdogan

School of Engineering and Electronics,
The University of Edinburgh,
Mayfield Road, Edinburgh, EH9 3JL, Scotland, UK
z.khan@ed.ac.uk

Abstract—Weight and size are the bottlenecks of portable wireless systems which are in turn dependent on area and power consumption of electronic systems. The situation becomes even worse if wireless systems are equipped with Multiple Input and Multiple Output (MIMO) technology which involves highly complex signal processing. This paper proposes an area and power efficient VLSI architecture for computing the pseudo inverse of augmented channel matrix used in MIMO systems. Results indicate 25% area and 24% power reduction compared to previous architecture in the literature without degrading the BER performance.

1. INTRODUCTION

Multiple Input - Multiple Output (MIMO) wireless communication is a new technology that promises to remove the limits and frustrations of wireless networks by providing spectral efficiency near Shannon's bound [1]. MIMO multiplies range, reliability and data speed of existing wireless systems [2]. Because of its advantages, MIMO is entering into almost every wireless network such as CDMA2000, and WCDMA as example [2]. However, such benefits of MIMO come at the expense of highly complex signal processing which directly contributes to high power consumption [3].

In CMOS, sources of power consumption include short circuits, leakage currents and switching. The switching or dynamic power equation is described as

$$P = kC_L V^2 f \quad [4]$$

where k represents the switching activity factor, C_L the total physical capacitance, V the supply voltage and f the frequency of operation. Algorithmic power optimization includes reduction of both physical capacitance and switching activity factor. Physical capacitance can be reduced by reducing the area of hardware through efficient implementation [5]. Switching activity reduction either comes from area reduction that reduces the number of nodes or from reducing switching frequency of nodes. One of the algorithmic optimizations is reducing redundancy [6] from a design. By reducing the redundant operations or hardware,

unnecessary switching of the clock as well as other signals can be avoided, thereby saving power consumption.

VBLAST (Vertical Bell Labs Layered Space Time) is a MIMO detection algorithm [7] that provides a good trade-off between BER (Bit Error Rate) performance and computational complexity compared to its counter parts. Zero Forcing (ZF) and Minimum Mean Square Error (MMSE) detectors [8] are computationally less expensive than VBLAST; however, they provide poor BER performance compared to VBLAST. The optimal solution is maximum likelihood (ML) [8] detection which provides best BER performance. However, it is highly expensive regarding computational complexity. This increases exponentially with the number of antennas used and is prohibitively high for antennas more than 4. Therefore, the ML algorithm cannot be implemented on mobile platforms due to its high overhead of area and power [3].

VBLAST can provide BER performance close to ML at a computational complexity much less than ML [8]. In VBLAST itself, the bottlenecks are repeated pseudo inverse calculation required to compute optimal ordering and nulling vectors.

The pseudo inverse can be computed using the complex singular value decomposition method (SVD) [9]. However, pseudo inverse computation through SVD is expensive both in silicon and power consumption. For equal transmit and receive antennas ($M=N$), the complexity of pseudo inverse through SVD in MMSE-VBLAT is $(27/4)M^4$ [10]. The complexity grows as the fourth power of M which is quite huge. The square root algorithm [10] not only computes pseudo inverse but also avoids repeated pseudo inverse computation and reduces the computational complexity of VBLAST to $O(M^3)$ without degrading performance [10].

The only VLSI architecture for computing a pseudo inverse module through the square root algorithm has been devised in [11] in which a 3-CORDIC based supercell proposed in [12] has been used. The architecture presented in [11] is a straight forward implementation without regard to area and power optimizations. The architecture proposed in this paper for pseudo inverse computation exploits the

parallelism inherent in Jacobi's rotation and is different and better from the architecture in [11] in that it uses two independent and generic pipelined CORDIC units instead of three [11], thereby saving area and power. The scale correction in CORDIC units in the proposed architecture is carried out through 4 shifters and an adder instead of a 16-bit multiplier thereby saving area and power in scale correction as well as infinitesimal error. In addition to these algorithmic modifications to reduce redundancies as much as possible, the inputs to the idle modules are held at their previous states as long as they remain idle to avoid unnecessary switching. The rest of the paper is organized such that section 2 describes MIMO signal model and square root algorithm, section 3 explains the previous while section 4 describes proposed architectures. Section 5 provides results and section 6 concludes the paper.

2. MIMO SYSTEM MODEL AND SQUARE ROOT ALGORITHM FOR VBLAST

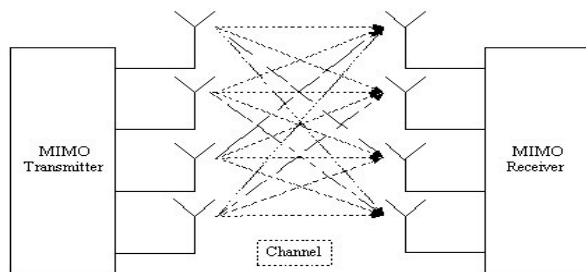


Figure 1: (MIMO System Model)

In MIMO communication system, more than one antenna are used at the transmitter to transmit symbols and more than one antenna are used at the receiver to receive them. There are two types of techniques used in MIMO, the first is spatial multiplexing in which the symbols are de-multiplexed among transmit antennas and then transmitted simultaneously. These symbols are then received through multiple antennas. In the second case, space time coding is used and the symbol and its coded replica are transmitted from the multiple antennas. In the diagram of Figure 1, spatial multiplexing is used and M transmit antennas transmit M symbols simultaneously while each symbol is received by the N receive antennas. Each symbol transmitted is received by all the receiving antennas thus making multiple channel paths. These paths if combined make a matrix of channel elements. Each symbol makes N channel paths and is received by N receive antennas. Since there are M symbols transmitted simultaneously, the channel becomes a $N \times M$ channel matrix. Channel matrix inversion is needed to recover the transmitted signal. Channel inversion is done through the square root algorithm [10]. This algorithm is developed for MMSE-VBLAST and computes the QR decomposition of the augmented channel matrix given by

$$\begin{bmatrix} H^{N \times M} \\ \sqrt{\alpha} I^{M \times M} \end{bmatrix} = QR = \begin{bmatrix} Q_a^{N \times M} \\ x \end{bmatrix} R^{M \times M} \quad (5)$$

here x denotes the entries that are not relevant. A more detailed description about the algorithm is available in [10].

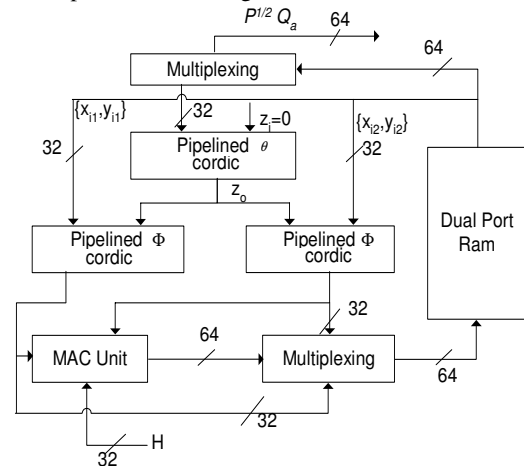


Figure 2: (VLSI architecture for pseudo inverse [11])

3. PREVIOUS PSEUDO INVERSE MODULE AND ITS LIMITATION

Figure 2 presents the architecture proposed in [11]. The architecture uses a supercell based on three n -stage pipelined CORDIC units. Ideally for a m -bit wordlength the number of micro-cells in the CORDIC module should be m . However, through experiments with the CORDIC, it was found that 13 micro-cells provide sufficient accuracy for pseudo inverse computation and n is chosen to be 13 for the CORDICs used in both the previous and the proposed pseudo inverse modules. Out of the three CORDICs, the top one is called the θ -CORDIC and operates only in vectoring mode to calculate the angle of rotation whereas the remaining two are called Φ -CORDICs and are used together to perform Jacobi rotation. The architecture is developed for a $M=N=4$ MIMO system.

The computation starts by calculating angles using the θ -CORDIC. When the pipelined θ -CORDIC is busy in calculating angles (M angles in pipe), the remaining $M-n$ cells (stages) of θ -CORDIC as well as all micro-cells of the two Φ -CORDICs are idle and consume unnecessary power. In rotation mode, when Φ -CORDICs are busy in vector rotation, approximately all micro-cells of θ -CORDIC as well as some cells of the Φ -CORDICs are idle and consume power. Initially 4 angles need be calculated to make the imaginary parts of the 4 leaders equal to zero. After applying all four leaders to the θ -CORDIC, the calculation of the 4

angles will occupy four micro-cells at a time. Other cells of θ -CORDIC as well as all cells of the Φ -CORDICs are idle. After making imaginary parts equal to zero, the process of zeroing the leaders is started which for a 4×4 system is performed using the parallel Jacobi's iteration. In the first iteration, two micro-cells of the θ -CORDIC (after inputs are applied) are performing the angle calculation while all others remain idle. In the second and third iteration, only one angle need be calculated at a time and therefore, only one micro-cell is busy while all others are idle. This clearly indicates that for this particular application, θ -CORDIC is most of the time idle and if the other two CORDICs are used for angle calculation, θ -CORDIC can be made redundant.

The Φ -CORDICs have to wait till the θ -CORDIC calculates the angle. Once the Φ -CORDICs receive the angle, they start rotation of the vectors. Similarly θ -CORDIC has to wait till rotated vectors come out of the Φ -CORDICs. Therefore, if θ -CORDIC is removed and both vectoring and rotation are performed through the two Φ -CORDICs, it is expected to achieve both area and power reduction. The latency will not be affected as explained already that rotation starts after completion of vectoring. The latency of both vectoring and its corresponding rotation will be the same in both cases. The difference is the use of the same hardware to perform both vectoring and rotation.

4. PROPOSED PSEUDO INVERSE MODULE

The proposed architecture for the pseudo inverse (Figure 3) consists of two independent and generic pipelined CORDICs and a dual port ram to support the two CORDICs. Each CORDIC is developed to have 13 micro-cells. The number system used is $16Q8$ with 8 bits for precision, 7 bits for dynamic range and 1 bit for sign. The process of computing the pseudo inverse is the same as described in section 3; however, the difference is that the two CORDICs are used both in vectoring as well as in rotation mode. The control unit of each micro-cell is designed to configure the cell for either vector or rotation mode. The inputs to the control unit (Figure 4) of each micro-cell are the sign bits of x , y and z inputs as well as CORDIC mode signal. The CORDIC mode signal determines the vectoring or rotation mode for the micro-cell. This signal is propagated together with x , y and z data from the first micro-cell to the last one. Initially the two CORDICs are in the vectoring mode and calculate the angles. The angles are then applied as input to both CORDICs and both CORDICs perform rotation together in the way described in section 3. The rotated vector needs scale correction in which each coordinate of the rotated vector is multiplied with the scale correction constant which is 0.6057 [12]. If this is done using a conventional 16-bit multiplier as is used in the previous architecture, it will be costly both in area as well as in power. A simple shift and add circuit (Figure 5) will perform scale correction. The scale correction in $16Q8$ format is 10011011 which is equal

to $2^7 + 2^4 + 2^3 + 2^1 + 2^0$ and can be implemented as in Figure 5. Here \ll represents left shift.

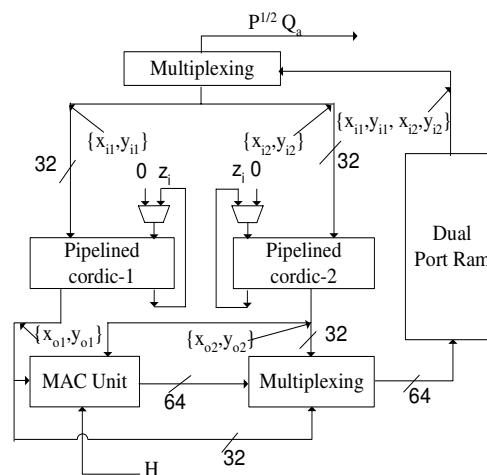


Figure 3: (Proposed pseudo inverse module)

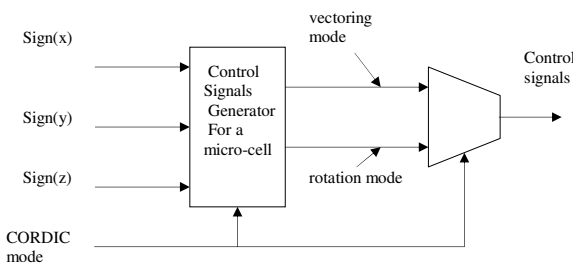


Figure 4: (Control Unit for a micro-cell)

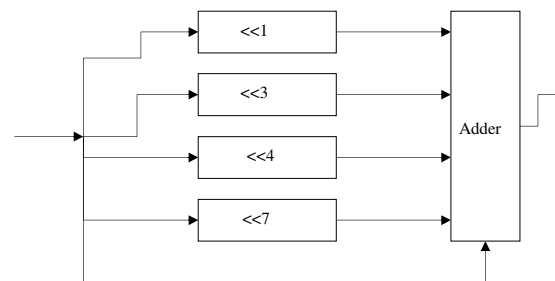


Figure 5: (Scale Correction using shifters and adder)

5. SIMULATION AND SYNTHESIS RESULTS

The proposed and previous pseudo inverse modules are simulated within MMSE-VBLAST environment modeled in MatLab. The results of the high level model show no degradation in BER performance in the case of proposed architecture. The proposed and the previous [11] pseudo inverse architectures have been synthesized using Synopsys Design Compiler and mapped to 0.18um CMOS technology.

The area comparison is given in Table 1 which shows a saving of about 25.2% over the previous architecture. The proposed and previous architectures have been simulated at 100MHz for power comparison which is recorded in Table 2. From the architecture, it is clear that CORDIC and multipliers (both in scale factor correction as well as in MAC unit) are the major power consuming units. Eliminating one CORDIC unit as well as replacing multipliers in scale correction by shift and add sequence have reduced the power consumption in the proposed architecture by 32%. The control unit of the proposed architecture consumes more power compared to the control unit of the previous architecture because of its increased complexity in generating control signals. It can be noted that CORDIC-2 in the proposed architecture consumes less power compared to CORDIC-1 due to the reason that it remains idle for more clock cycles as compared to CORDIC-1 and during that period switching activity is kept at minimum by holding the inputs to the cells at the previous value. The area and power can be reduced further by reducing the number of multipliers in the MAC unit. It should be noted that existing MAC unit has four multipliers in both architectures to perform complex multiplication.

6. CONCLUSION

The authors have presented an area and power efficient VLSI architecture for computing pseudo inverse through square root algorithm. The architecture reduces area and power consumption by reducing the redundant hardware as much as possible and achieves 25% area and 24% power efficiency. The architecture exploits parallelism inherent in Jacobi's rotation. The architecture is simulated within MMSE-VBLAST system and imposes no degradation in performance as well as latency.

8. REFERENCES

[1] G. J. Foschini, "Layered Space-Time architecture for wireless communication in fading environments when using multiple antennas," Bell Labs Tech. J., vol 2, Autumn 1996

[2] G. Lawton, "Is MIMO the future of wireless communications?", computer, vol: 37, issue 7, July 2004 Pages 20-22

[3] D. Garrett, L. Davis, St. Brink, B. Hochwald, G. Knagge, "Silicon complexity for maximum likelihood MIMO detection using spherical decoding", Solid-State Circuits, IEEE Journal, vol. 39, Issue 9, Sept. 2004, Pp(s):1544-52

[4] M. Chandrakasam, M. Potkonjak, R.Mehra, J. Rabaey, and R. Broderson, "Optimizing power using transformations", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no.1 pp. 12-31, January 1995

[5] M.Pedram,"Power Minimisation in IC Design: Principles and Applications", ACM Transactions on

Design Automation of Electronic Systems, vol. 1, no. 1, pp. 3-56, January 1996.

[6] X. Wu, M. Pedram, L. Wang, "Multi-code state assignment for low power design", Circuits, Devices and Systems, IEE Proceedings vol. 147, Issue 5, Oct. 2000 Page(s):271 - 275

[7] P.W. Wolniansky, G.J. Foschini, G.D. Golden, and R.A. Valenzuela, "V-BLAST: an architecture for realizing very high data rates over the rich-scattering wireless channel", Proc. ISSSE'98, Sept. 1998

[8] A. Adjoudani, E.C. Beck, A.P. Burg, G.M. Djuknic, T.G. Gvoth, D. Haessig, S. Manji, M.A. Milbrodt, M. Rupp, D. Samardzija," Prototype experience for MIMO BLAST over third-generation wireless system", Selected Areas in Communications, IEEE Journal on Vol. 21, Issue 3, April 2003 Page(s):440 - 451

[9] Gene. H. Golub, Charless F. Van Loan, "Matrix Computation"

[10] B. Hassibi, "An efficient square-root algorithm for BLAST", Acoustics, Speech, and Signal Processing, 2000. ICASSP '00. Proceedings. 2000 IEEE International Conference on, Volume 2, 5-9 June 2000 Page(s):II737 - II740 vol.2

[11] Z. Guo, P. Nilsson, "A VLSI implementation of MIMO detection for future wireless communications", Personal, Indoor and Mobile Radio Communications, 2003. PIMRC 2003. 14th IEEE Proceedings on, vol. 3, 7-10 Sept. 2003 Pages:29-49

[12] C.M. Rader, "VLSI systolic arrays for adaptive nulling", (radar) Signal Processing Magazine, IEEE , vol. 13 , Issue: 4 , July 1996, Pages:29 - 49

| | Previous pseudo inverse module | Area μm^2 | Proposed pseudo inverse module | Area μm^2 |
|---|--------------------------------|----------------------|--------------------------------|----------------------|
| 1 | Θ CORDIC | 250120 | CORDIC-1 | 253659 |
| 2 | Φ CORDIC | 258920 | CORDIC-2 | 253659 |
| 3 | Φ CORDIC | 258920 | ----- | ----- |
| 4 | MAC Unit | 147611 | MAC Unit | 147611 |
| 5 | Control Unit and duram | 49210 | Control Unit and duram | 66015 |
| | Total | 964781 | Total | 720944 |
| | | | Percent Saving | 25% |

Table 1: (Area Comparison of the two architectures)

| | Previous pseudo inverse module | Power mW | Proposed pseudo inverse module | Power mW |
|---|--------------------------------|----------|--------------------------------|----------|
| 1 | Θ CORDIC | 31.278 | CORDIC-1 | 33.608 |
| 2 | Φ CORDIC | 33.548 | CORDIC-2 | 29.409 |
| 3 | Φ CORDIC | 33.463 | ----- | ----- |
| 4 | MAC Unit | 28.484 | MAC Unit | 28.449 |
| 5 | Control Unit and duram | 12.225 | Control Unit and duram | 14.329 |
| | Total | 138.998 | Total | 105.795 |
| | | | Percent Saving | 24% |

Table 2: (Power Comparison of the two architectures)