

A Multi-objective Genetic Algorithm for On-chip Real-time Adaptation of a Multi-Carrier based Telecommunications Receiver

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Abstract

This paper presents a multi-objective algorithm for on-line adaptation of a multi-carrier code-division multiple access (MC-CDMA) receiver. A specially tailored Genetic Algorithm (GA) is developed in order to adapt the complete receiver while dynamically optimizing the critical Fast Fourier Transform (FFT) section of the receiver for both error value and power consumption. The results obtained, through evaluation within complete receiver architecture, demonstrate that the algorithm can find results optimized for both objectives. Results also show that there are significant reductions in error value and power consumption as compared to the reference solution.

1. Introduction

Multi-carrier code division multiple access (MC-CDMA) is one of the most attractive wireless protocols for broadband multimedia communication system. It combines the advantages of orthogonal frequency division multiplexing (OFDM) and code division multiple access (CDMA) to produce a spectrally efficient multi-user access system. The combined requirement for high performance and power is the critical design issue for these wireless systems [1]. These systems must have high performance (in terms of smaller error) at their outputs as they operate in changing environments such as indoor/outdoor, stationary/moving, etc. This implies changes in data rate and bit error rate along with changing bandwidth and other channel parameters such as delay spread. On the other hand, the portability requirement of these systems is mainly responsible for the need for low power consumption. In a MC-CDMA receiver, Fast Fourier Transform (FFT) block is one of the most power consuming units. One way to reduce the power consumption here is by dynamically reducing the

complexity of the receiver architecture in real time as per the changing channel requirements such as the delay spread, signal to noise ratio (SNR), bandwidth and bit error rate [1]. It is therefore important to design systems which can adapt their operations instead of being designed for the worst case scenario.

This paper presents a multi-objective algorithm for on-line adaptation of a MC-CDMA receiver. A specially tailored GA is developed in order to adapt the complete receiver while dynamically optimizing the critical FFT section of the receiver for both error value and power consumption. The results obtained, through evaluation within complete receiver architecture, demonstrate that the algorithm can find results optimized for both objectives. Results also show that there are significant reductions in error value and power consumption as compared to the reference solution.

The paper presents the analysis of the impact of word length optimization of fixed-point Fast Fourier Transform (FFT) coefficients on error and power consumption using a non-dominated sorting based GA (NSGA) [2]. GA [3] is used in this optimization because it is a class of evolutionary algorithm that can be used for the discovery of near-optimal solutions to multi-modal problems. It makes use of population of solutions, enabling simultaneous discovery of multiple solutions. The work investigates the possibility to find a solution for the FFT coefficients which have optimum performance in terms of error and power consumption as compared to the reference solution. A specific issue of concern in this research would be targeting on-chip optimization of a complete wireless MC-CDMA receiver.

2. MC-CDMA receiver

A MC-CDMA receiver consists of two main blocks, an FFT block to demodulate the OFDM signals and a

combiner block which equalizes the signal and separates out the coded users. The FFT processor is one of the blocks which contribute the most power consumption [1]. Power consumption of FFT processor depends on the size of the word length of the data and the FFT coefficients [4]. The larger word length means the higher power consumption which is due to more switching activities [5]. On the hands, larger word length means less error and higher signal to noise ratio (SNR).

The FFT processor used in this work is based on the radix-4 single-path delay commutator (R4SDC) architecture proposed by the authors in [6]. This architecture is chosen because it has tremendous saving in hardware and power consumption for real-time applications [7].

3. Multi-objective Genetic Algorithm (GA)

Multi-objective GA is crucial in order to optimize multiple fitness measures in many real world problems with multiple conflicting objectives [2]. In multi-objective optimization, there is a possibility that more than one optimal solution is obtained. A set of optimal solutions is called a Pareto-optimal set. This is the main difference between multi-objective optimization and single-objective optimization.

In this work, a NSGA is used to optimize the word length of the fixed-point FFT coefficients for two objectives.

(1) Coefficients: they should have smallest total error as possible and,

(2) Power consumption: the complete receiver must have the lowest power consumption. These two objectives conflict with each other, as an increase in the word length will reduce the error but increases the power consumption. Fitness evaluations for the error and power consumptions are explained in details in sections 3.3 and 3.4 respectively.

3.1 System Description

Figure 1 shows the block diagram of the targeted system which consists of three main blocks namely, memory, microprocessor, and reconfigurable MC-CDMA receiver. The choice of the microprocessor is an OpenRISC 1200. This is a common MIPS-based architecture which has been used for a spectrum of implementations at a variety of price/performance levels for a range of industrial telecommunication applications [8]. The main function of the microprocessor is executing the adaptation algorithm to find solutions of the optimized FFT coefficients for a specific word length. This is then propagated through

the complete receiver. The memory is used to store the adaptation program and the chromosomes.

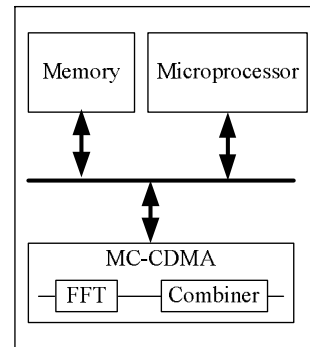


Figure 1. Block diagram of the system

3.2 Chromosome

Figure 2 displays the chromosome representation of the coefficients for the whole FFT processor. Each stage of the chromosome contains 2 fields of information: coefficients and control. The coefficients field stores the real and imaginary parts of the FFT coefficients (twiddle factor), W_N and data coefficients, $x(n)$. First stage is the only stage which has both W_N and $x(n)$ coefficients. The other stages only have the FFT coefficients except for the final stage. All the coefficients are initially 16 bits in length. The control bits are used to select either FFT coefficients optimization or data optimization or both of these.

The length of the chromosome depends on the size of the FFT. For an example, a 16-point FFT will consist of 16 FFT coefficients and 16 data coefficients in the first stage. The initial data and FFT coefficients are obtained from the MATLAB FFT procedure and then are represented as 16-bit numbers. A population size of 50 is chosen through experimentation as it provides sufficient solution diversity.

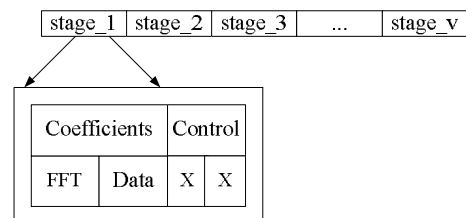


Figure 2. Chromosome structure

3.3 Error Fitness Evaluation

Figure 3 illustrates the methodology used to evaluate the error fitness. Initially, with a sequence of

input data, $x(n)$ and 16-bit FFT coefficients, the FFT processor calculates the outputs, $X_1(k)$. Next, with the same $x(n)$ and with the optimized FFT coefficients, the FFT processor again calculates the outputs, $X_2(k)$. Both outputs are then compared for error calculations, $e(k)$. The corresponding SNR(k) for all the FFT outputs are then calculated using the formula in (1).

$$SNR = 10 \log_{10} \left[\frac{(R_{16})^2 + (I_{16})^2}{(R_{16} - R_{wl})^2 + (I_{16} - I_{wl})^2} \right] \quad (1)$$

R_{16} , I_{16} , R_{wl} and I_{wl} are the real and imaginary parts of the FFT output before and after optimization respectively. Next, each SNR(k) value is compared with a target, SNRT. If the former is lower than the latter, an error will be calculated as the difference between the latter and the former. Finally, the total error is calculated by summing the all individual errors.

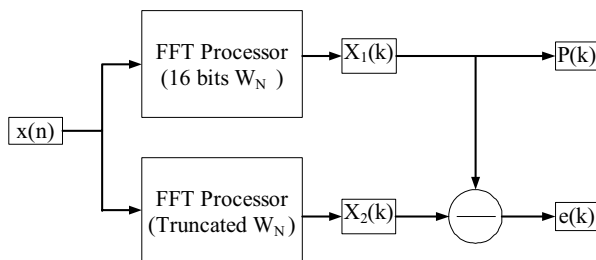


Figure 3. Methodology to evaluate error fitness

3.4 Power Fitness Evaluation

Power evaluation is performed by calculating the sum of switching activity based on hamming distance in the FFT coefficients using a specific word length. It can be shown that, switching power, P_{sw} , is the main source of power consumption in a typical CMOS logic gate. Equation (2) illustrates how switching power is calculated.

$$P_{sw} = \frac{1}{2} k C_{load} V_{dd}^2 f \quad (2)$$

V_{dd} is the supply voltage, f is the clock frequency, C_{load} is the load capacitance of the gate, k is the switching activity factor which is defined as the average number of times the gate makes an active transition in a single clock cycle. If, C_{load} , V_{dd} and f are constants, then P_{sw} will be directly proportional to the k .

4. Results

In this work, the multi-objective Genetic Algorithm is used to adapt the FFT coefficients in the first stage of the FFT processor at word lengths of 10, 11 and 12 bits. The results are compared with a reference solution

in terms of switching activity and total error. The reference solution is obtained by truncating all the undesired bits of the FFT coefficients. This is an easier and less complex method to reduce the word length [4]. Table 1 displays the figures of total error and switching activity for the reference solution. These figures are obtained using error fitness and power fitness evaluations as explained in sections 3.3 and 3.4 respectively with the chosen SNRT value of 80 dB. The table shows that as the word length increases, the switching activity increases and the total error decreases.

Table 1. Error and switching activity of reference solution

Word length	Switching Activity	Total Error (dB)
10 bits	404	1630
11 bits	462	1195
12 bits	502	711

Figure 4 shows the best GA search results for the 10-bit word length from five runs. In this experiment, the maximum limit for the switching activity and total error are set to 404 and 1630 dB respectively according to the values indicated in Table 1. The figure shows that the GA can find many solutions which meet both objectives.

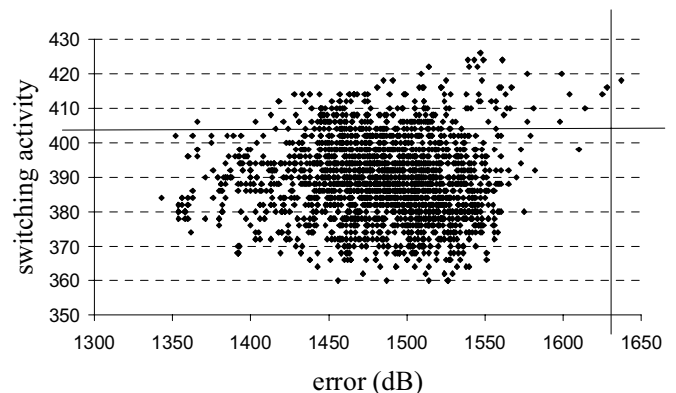


Figure 4. GA search results for 10-bit word length

Table 2 lists the Pareto-optimal set for this search which includes the number of generation in which the solution is found, the reduction in switching activity and total error. The maximum reduction in switching activity and total errors are 11% and 18% respectively.

Table 2. Pareto-optimal set for 10-bit optimization

gen	Switching Activity	Reduction (%)	Total Error (dB)	Reduction (%)
1361	384	5	1343	18
1352	378	6	1354	17
1353	374	7	1362	16
1378	368	9	1392	15
2226	360	11	1456	11

Figure 5 illustrates the best GA search result for the second experiment on optimization with 11-bit word length obtained after five runs. The maximum limits for the switching activity and total error are set to 462 and 1195 dB respectively based on the values in Table 1. The figure shows that the GA is also able to find many solutions which meet both objectives. One of the solutions from the Pareto-optimal set which is found in the 945th generation has the figures for switching activity and total error of 416 and 1028 dB respectively. This implies that the solution is 10% and 14% better than the reference solution in terms of switching activity and total error respectively.

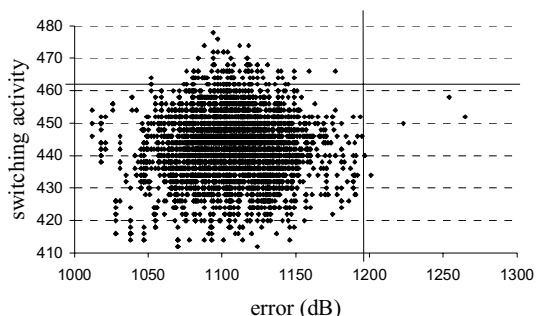


Figure 5. GA search results for 11-bit word length

The GA is also able to find many solutions which meet both objectives in the third experiment on optimization for 12-bit word length. One of the solutions from the Pareto-optimal set which is found in the 709th generation has the switching activity and total error figures of 422 and 632 dB respectively. This implies that the solution is 11% and 16% better than the reference solution in terms of switching activity and total error respectively.

5. Conclusion

In this paper we have presented a multi-objective Genetic Algorithm based on non-dominated sorting for

on-chip real-time adaptation of a multi-carrier receiver used in numerous telecommunication applications. Although the adaptation targets the Fast Fourier section (as this is the most critical block within the receiver), the evaluation is performed on the complete receiver architecture. Results show that the algorithm can find solutions which have significant reductions in error and switching capacitance compared to a reference solution.

6. References

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