

# A RECONFIGURABLE VITERBI TRACEBACK FOR IMPLEMENTATION ON TURBO DECODING ARRAY

Imran Ahmed<sup>\*†</sup>

Tughrul Arslan<sup>\*†</sup>

<sup>\*</sup> School of Electronics and Engineering,  
University of Edinburgh, King's Buildings  
Mayfield Road, Edinburgh, EH9 3JL, UK  
email: imran.ahmed@sli-institute.ac.uk

<sup>†</sup> Institute for System Level Integration, The  
Alba Campus, The Alba Centre, Livingston,  
Scotland, EH54 7EG, UK  
email: T.Arslan@ed.ac.uk

## ABSTRACT

The trace back operation as used in Viterbi decoding is presented. The trace back is used for a new large constraint length, soft decision viterbi decoder designed to be implemented reusing components of turbo decoding array. The viterbi decoder can be reconfigured for standards such as CDMA2000, WCDMA (UMTS), ADSL, IEEE 802.11 and GSM. The proposed trace back operation supports all of these multiple standards. The viterbi decoding is made reconfigurable between different trellis types, constraint lengths and rates that can be reconfigured for the desired standard. The reconfigurable fabric is implemented as a subset of turbo decoder array on a 180 nm UMC process technology.

## VLSI DESIGN

The main aim of this reported research is to present the viterbi trace back operation used in an open trellis structure for a unified viterbi and turbo decoding for multiple standards. The viterbi components of the architecture can support up to 256 states, trellises with different generator polynomials and rates.

In contrast to state serial [1,2] and fully parallel architectures [3] our viterbi design uses an intermediate solution. A better area and speed efficiency can be achieved by Processing N states (up to 256) by using P Add-Compare-Select 'ACS' units (P=8) [3]. The survivor memories and their management with reconfigurable trace back approach are presented in the subsequent sections.

### 1.1. Path History (PH) Memory.

Path History Memory is used in Viterbi algorithm to find the survivor path. The contents of this memory are updated on each stage 'L' of the trellis which allows reconstructing the survivor path. There are 8 ACS units in the array that output 8 decision bits per clock cycle. These decision bits (survivor states) are saved in the PH RAM. Total size of the PH RAM is given by:

Size of PH RAM =  $(2^{L-1}/2^M) \times WL \times \text{total windows}$  ---- (1)  
--- where WL (window length) is 5-6 times the constraint length. 'L' is the constraint length and M=3 for 8 ACS units. The total processing of states ( $2^{L-1}$  states) is done by a smaller de Bruijn graph of  $2^M$  states. For example in equation (1), the size of the PH RAM for constraint length 9 (as in 3GPP) will be:

Size of PH RAM =  $32 \times 54 \times 4 = 6912 \times 8$  bits.

There is 8K (2Kx8) of output RAM available in turbo decoding array [4]. This is reused for PH Memory and is shown in the figure 1.

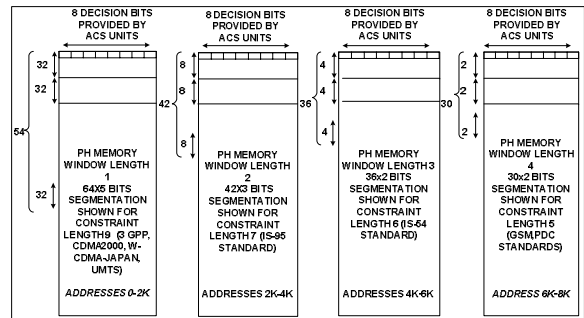


Figure 1. 2Kx4 identical path history RAMs, Segmentation and mappings shown for different standards.

Each block of 2K RAM is used to store one window length (WL) of decision bits. These RAMs are segmented by total states of the trellis. For example, for 256 states there are 256 decision bits (one for each state). Therefore the RAMs will be divided into  $32 \times 8$  wide segments. The total number of segments will be equal to one window length (constraint length  $\times 6 = 54$  for 3GPP). Figure 1 and table 1 show these mappings and segmentation for various standards. PH memory is read by trace back processors as they calculate the survivor path in the reverse traversing of the trellis.

Standard	Const. length	Memory utilization for each 2K RAM = WL x segment size.
W-CDMA(Japan) CDMA 2000 UMTS	9	$54 \times 32 = 1728 \times 8$ bits
GSM, PDC	5	$30 \times 2 = 60 \times 8$ bits
IS-95, IEEE 802.16	7	$42 \times 8 = 336 \times 8$ bits

IS-54	6	36 x 4 = 144 X 8 bits
-------	---	-----------------------

Table1. Memory utilization for different standards.

### 1.2. Reconfigurable Trace Back Processing.

The input/output state connections for the ACS blocks are explained in figure 2. Total number of states =  $2^{a+1}$ .

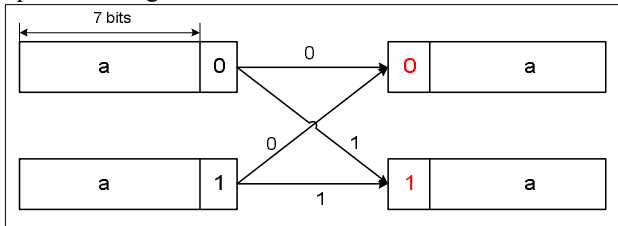


Figure 2. Next and Previous state calculation for all trellises

For example if the state at stage ‘L’ of trellis is 0\_111111 (figure 3); it implies that the decoded bit (shown in red) is 0 and the two possible states connected to this winning state at stage ‘L-1’ of trellis are 111111\_0 and 111111\_1. The previous winning state decisions are provided by PH RAMs. These were stored in PH RAMs during the ACS calculations.

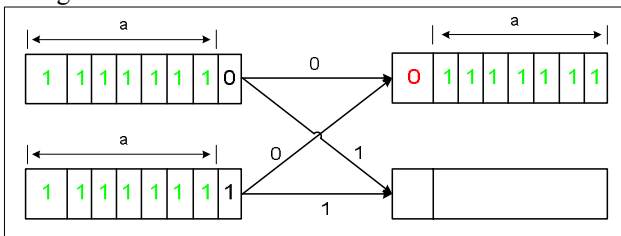


Figure 3 Example showing previous state calculation  
There are two reverse processors B1 and B2 (dummy) working in parallel, each accessing separate PH RAM. B2 calculations initialize the start state of B1 To get the survivor path, we have chosen the trace back technique as register exchange in not preferred for large constraint lengths [5].

As explained above, the previous trellis path stage  $S_{L-1}$  is given by the current path state  $S_L$  according to the following update.

$$S_{L-1} = [S_L \ll 1, D]$$

which corresponds to a left shift of the current state introducing the value of surviving bit D in the vacant position. This is also shown by D1-D7 in figure 4. Survivor bit is selected by multiplexer M1 from the data bus of PH Memories. The select control to this multiplexer is provided by D1, D2, D3 outputs. 6 bit Down Counter is initialized with the last address of PH Memory and counts down by 1. The decrement in count provides jump of one segment length. Reverse processor B1 and B2 share the same counter and shifter.

Reconfigurable trace back processing is explained with examples of 3GPP and GSM in table 2.

Let  $U_4\_U_3\_U_2\_U_1\_U_0$  are outputs of buffers B1-B2\_B3\_B4 and  $C_6\_C_5\_C_4\_C_3\_C_2\_C_1\_C_0$  are the outputs of the 6 bit down counter. Output of the arithmetic shifter with zero shift is 0 0 0 0 C6 C5 C4 C3 C2 C1 C0.

	B1	B2	B3	B4	B5	B6	B7	B8
GSM	On	on	on	On	On	Off	On	On
3GPP	Off	Off	off	Off	Off	On	Off	Off

Table 4. Tri state buffer controls for reconfigurable trace back processing

The contents of the read register for 3GPP using the controls in table 4 and table 5 will be

0	0	C6	C5	C4	C3	C2	C1	C0	U1	U0
---	---	----	----	----	----	----	----	----	----	----

By a similar reasoning the read register contents for GSM are:

C5	C4	C3	C2	C1	C0	U4	U3	U2	U1	U0
----	----	----	----	----	----	----	----	----	----	----

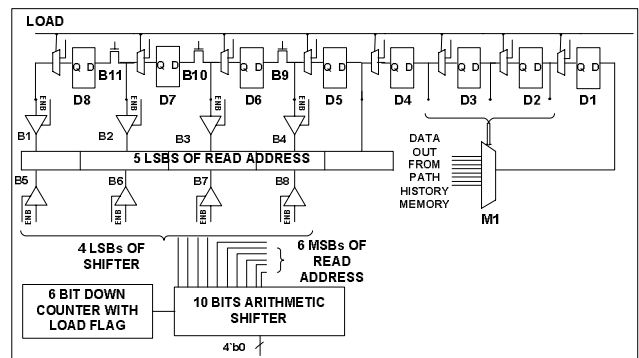


Figure 4. Traceback processing

Virtual Silicon 2K x 8 synchronous (separate read and write port) macro RAMs were used for Path history memory consuming 110 uW/MHz/Port. The decoder consumes 69mw at 20MHz occupying 2.824 mm<sup>2</sup> area.

## 2. REFERENCES

- [1] Inyup Kang, et. al., “Low-Power Viterbi Decoder for CDMA Mobile Terminals,” *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 473–482, Mar. 1998.
- [2] S. C. Glinski, et. al., “A processor for graph search algorithms” in Proc. ISSCC’87, New York, 1987, pp. 162–163.
- [3] C. Y Chung and K. Yao, “Systolic array processing of the Viterbi algorithm,” *IEEE Trans. Inform. Theory*, vol. 35, no1, pp. 76-86, Jan 1989.
- [4] I. Ahmed, T. Arslan, “Improved Memory Strategy for LogMap turbo decoders,”. SOC Conference, 2005. Proceedings IEEE international pages 103-104, Sept 25-28 2005
- [5] C.M. Rader, “Memory management in a Viterbi decoder,” *IEEE Trans. Commun.*, vol. COM-29, pp. 1399-1401, Sept. 1981.