

Modulator implementation: The modulator was implemented with a 0.35 μm CMOS technology utilising fully differential SC structures. The size of the modulator was $1.3 \times 1.0 \text{ mm}^2$. The targeted modulator resolution was 14 bits with $OSR = 32$, and approximately two bits were reserved for various nonidealities. The target for the sampling rate was specified to be 50 MHz.

OTA is the most critical component for the performance of the modulator. Thus, a low-voltage, high-speed complementary folded cascode feedforward compensated OTA [7] was designed with an efficient optimisation algorithm, presented in [8]. The main demands were low voltage ($\sim 2.5 \text{ V}$ at 4 mA bias currents), high-speed ($> 450 \text{ MHz}$ unity-gain frequency (10 pF load capacitance)), low noise, sufficient gain ($> 65 \text{ dB}$), slew rate, linearity, and good stability ($> 45^\circ\text{--}60^\circ$ phase margin). Also, other components, such as the one-bit quantiser (comparator) and three-bit A/D and D/A were optimised for high-speed and low-voltage operation. In order to obtain the maximum benefit from the high-speed components, pipelining and specific eight-phase clocking strategies were utilised effectively by allowing as much settling time for the components as possible, but avoiding the switch charge injection problems. The details of the circuit design are presented in [9].

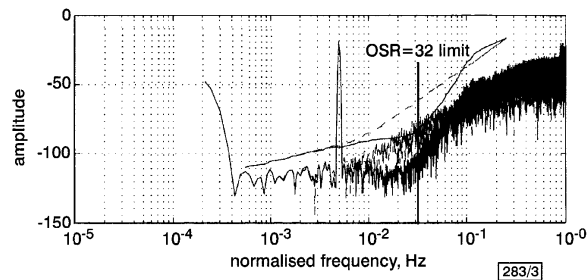


Fig. 3 Measured spectra and cumulative summed noise powers of second- and fourth-order sigma-delta modulators

--- second-order modulator
— fourth-order modulator

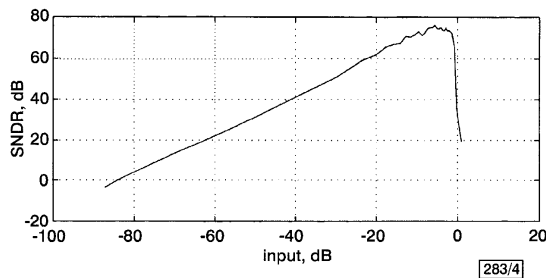


Fig. 4 Measured signal-to-noise and distortion ratio (SNDR) of fourth-order sigma-delta modulator

Measurement results: The modulator measurement environment consisted of a custom two-layer test printed circuit board (PCB), two signal generators, a logic analyser, and a personal computer (PC). The maximum internal operation frequency was limited by the time constant and the slew rate of the integrators, which also determined how accurately and linearly the samples settled at the end of the integration phase [9]. The measured noise shaping spectrum of the second- and fourth-order modulators together with their cumulative summed noise powers are presented in Fig. 3. The supply voltage was 2.5 V, sampling rate 50 MHz and the frequency of the sinusoidal input signal was 125 kHz. The FFTs were calculated from 32768 samples using the Kaiser window ($\beta = 20$) in order to prevent spectral leakage effects. The effect of the transmission zero can be seen as a knee in the cumulative summed noise power curve near $OSR = 32$. The measured SNDR curve as a function of the input signal amplitude is presented in Fig. 4. The experimental modulator chip operates in good agreement with the theory and the following performance values were measured at $OSR = 32$: $SNDR = 76 \text{ dB}$, $SNR = 85 \text{ dB}$, and the dynamic range (DR) = 83 dB. The modulator was observed to function up to a clock frequency of 150 MHz.

Conclusions: A low-voltage, high-speed, fourth-order sigma-delta modulator implementation has been presented. The modulator uti-

lises pipelining, multibit A/D and D/A converters, fully interstage scaling, and a transmission zero to improve the performance. Integrator scaling and coefficient optimisation guarantee robust operation and a compact layout. At the circuit level the clocking strategies and the circuit structures together with the developed optimisation methods made it possible to implement the modulator for high-speed and low-voltage operation. The measurement results of the experimental modulator chip demonstrated good agreement with the simulations.

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Programmable multiplierless digital filter array for embedded SoC applications

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The authors present a novel, programmable logic array for implementing high performance filter functions within embedded system-on-chip platforms. The novelty of the architecture is demonstrated through its specially tailored configurable logic units, and hierarchical routing scheme. The architecture and routing hierarchy are described using a filter example and results are provided demonstrating scalability, speed, and array utilisation using a typical SoC bus specification.

Introduction: With the advent of system-on-chip (SoC) devices, there is an increasing demand for high performance, dedicated, programmable digital signal processor (DSP) cores. These cores must be suitable for embedding in SoC platforms, for a wide range of applications. Finite impulse response (FIR) filters are used in many of these applications, ranging from audio data manipulation to channel equalisation. General purpose DSPs, such as the TMS320 series from Texas Instruments, do not provide sufficient throughput to implement high speed FIR filters, due to their single multiplier architecture. General purpose

FPGAs, such as those from Xilinx, are suitable for implementing dedicated filter architectures. However, the general functionality of FPGAs results in complex configurable logic blocks (CLBs) which require a high degree of interconnect. This restricts circuit throughput and increases the embedded filter core size within the total SoC platform area. Multiplierless filter design techniques have been shown to produce high performance architectures beyond those attainable through implementation on general purpose DSPs [1]. In recent years a configurable architecture has been proposed for the implementation of multiplier-free filters [2]. However, this architecture uses a single bus, which therefore produces a bottle-neck and restricts throughput. In addition, the size and complexity of the CLBs used severely limits the scalability of the architecture, as CLBs do not efficiently map into filter coefficients.

This Letter presents a novel programmable logic array (PLA) dedicated for implementing high performance multiplierless filters. A custom CLB architecture together with a fast and local interconnect hierarchy provides a high degree of flexibility for realisation of a given filter specification. The highly parallel nature of the PLA ensures that the architecture scales linearly with filter complexity. These characteristics make it ideal for implementation as an embedded core for adaptive applications where the architecture can be reconfigured with external hardware or software. Our investigations show that the PLA can realise practical filters whilst 20-40% of its architecture remains redundant. This provides a potentially fault-tolerant, adaptive system, suitable for deployment in hostile environments; and further distinguishes our PLA from other more general purpose DSP and FPGA architectures.

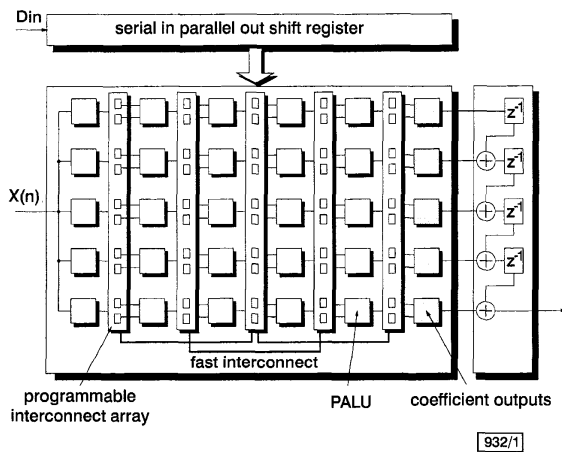


Fig. 1 System overview of programmable filter architecture

PLA architecture: A PLA core comprises five columns and six rows of programmable arithmetic logic units (PALUs). These dimensions were empirically derived so as to produce a flexible architecture with low signal latency. The final PALU column is used to output coefficient taps. The PLA therefore implements filters in the transposed direct form. Fig. 1 presents the PLA core architecture. Input $X(n)$, output $Y(n)$ and coefficient data widths are specified by the designer. Multiple PLA cores can be instantiated during parameterisation in order to produce a PLA architecture capable of implementing filters with a maximum of $5 \times N$ taps, where N denotes the number of PLA cores to be connected. PALUs are arranged in columns, each connecting to an array of programmable interconnect logic, which in turn connects to the next column of PALUs. A second level of fast interconnect provides greater connectivity between non-adjacent PALU columns through additional routing of alternate interconnect arrays. Interconnect arrays also provide each PALU with a direct connection to $X(n)$, and to logic '0'. An example of the hierarchical interconnect strategy can be seen in Fig. 2. Three bits of control logic are required to programme the interconnect for each PALU input. The entire PLA core is configured serially via a serial-in-parallel-out shift register.

PALU architecture: Fig. 2 also displays the structure of our PALU element. Each PALU is able to implement either a parallel

left-shift (SH), addition or subtraction (AoS). Bit width ' L ' is dependent on the input data width of ' $X(n)$ '. Five control bits are required to configure each PALU. The programmable shifter may left-shift from 0 to 3 bits, and requires a 2 bit control. A PALU implementing a shift-by-zero therefore acts as a through-connect. The first column of PALUs are left-shift only and are capable of shifting between 0 and $L - 2$ bits. Each PALU output connects to a synchronous register (R), creating a pipelined architecture to enable fast data throughput. A total of $C + 1$ clock cycles is therefore required before filtered data will be present on ' $Y(n)$ ', where $C = 6$ and is the number of PALU columns.

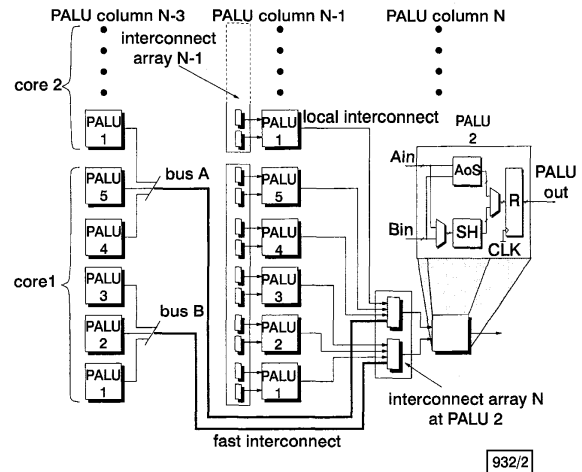


Fig. 2 Programmable routing between PALU elements showing local and fast connectivity

Design example: A number of practical filters have been implemented on our PLA. This Letter presents the implementation of a 20-tap Hilbert transformer, benchmarked by McClellan *et al.* in [3]. The filter was implemented on the PLA core in folded form and in 16-bit 2's complement. Two PLA cores were connected together in order to provide sufficient taps to implement the Hilbert transformer. The example PLA configuration can be seen in Fig. 3. Approximately 70% of the PALUs were required to implement the filter. This provides the PLA with sufficient free elements to be reconfigured should part of the architecture become damaged. Also, the throughput of the PLA is not affected by filter length. This is a considerable advantage over single multiplier filter architectures.

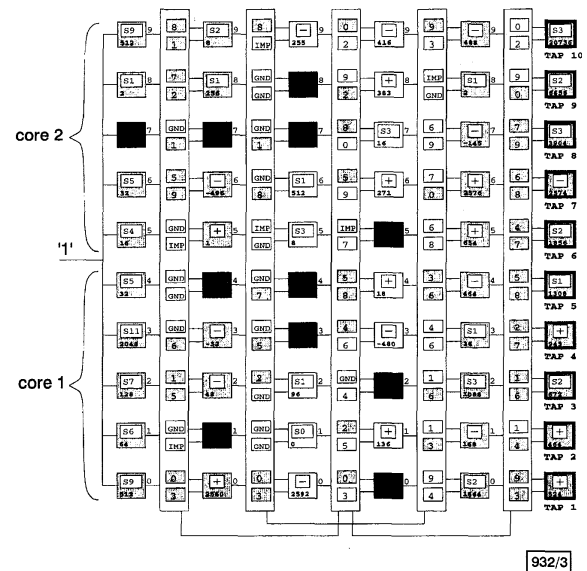


Fig. 3 Example PLA configuration for implementation of 20 tap Hilbert transformer

Blank PALUs show that logic is not used

Synthesis of PLA core: The PLA core has been synthesised from behavioural VHDL using the Synopsys Design Analyzer and Alcatel's 0.35 μm MTC45000 technology library. To determine the scalability of our PLA core, the architecture was synthesised at clock frequencies of 10, 25, 50, 80, 90 and 100 MHz, with all data widths set at 16 bits. These frequencies were chosen to reflect typical timing constraints required on high speed SoC bus architectures, which range from 60 to 100 MHz. The resulting logic area (in NAND gates) can be seen in Fig. 4. The area remains relatively constant up to 50 MHz. Between 50 and 100 MHz area increase is approximately linear. For technologies smaller than 0.35 μm , faster throughput could be achieved.

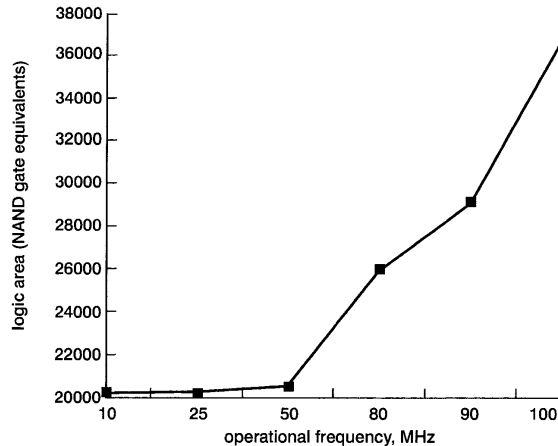


Fig. 4 Logic area of PLA core against synthesis for increasing operational speeds

■ synthesised area

Conclusions: We have presented a novel, high performance programmable logic array for the implementation of multiplierless digital filters. Coefficients are generated within a distributed, highly parallel architecture providing component redundancy, desirable in fault tolerant applications. High data throughput is achieved at speeds of up to 100 MHz and with a latency of seven clock cycles.

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Wideband low-distortion delta-sigma ADC topology

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A $\Delta\Sigma$ topology with reduced sensitivity to opamp nonlinearities is described. The technique is effective even for very low oversampling ratios, and can be used for any modulation order. Techniques for reducing other nonideal effects are also proposed.

Introduction: $\Delta\Sigma$ ADCs have been used predominantly in low bandwidth applications such as digital telephony and digital audio [1]. These applications rely on high oversampling ratios, typically between 32 and 256, to achieve the desired SNR and linear performance.

With the continuing advancement of technology, oversampled data conversion is becoming attractive for use in wideband applications, such as in xDSL modems and digital video. However, at very low oversampling ratios (for example, 4 or 8) required for such applications, these ADCs are increasingly sensitive to circuit imperfections, and require high-quality analogue components.

In this Letter, a second-order $\Delta\Sigma$ topology with low sensitivity to integrator nonlinearities is described. The technique is effective for any oversampling ratio, and can be applied to $\Delta\Sigma$ topologies of any order.

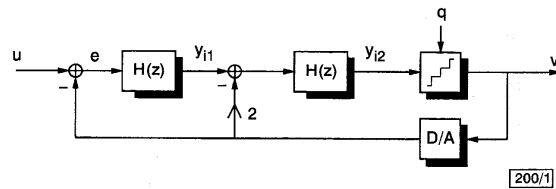


Fig. 1 Traditional topology

Distortion in traditional topology: Fig. 1 shows the topology of a traditional second-order $\Delta\Sigma$ modulator. The integrator blocks, denoted by $H(z)$, are typically realised as forward-Euler structures, i.e.:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (1)$$

In this structure, the quantisation noise q is filtered by a second-order highpass function. The signal transfer function, from the input u to the output v , is just a delay of two clock cycles, so $STF(z) = z^{-2}$.

The way distortion is created and processed in this topology will be explained next. The error signal e is the difference between the input u and the output v , and the $\Delta\Sigma$ loop tries to minimise this difference in the desired frequency band. However, the delay introduced by the STF causes e to contain a highpass-filtered version of the input signal u , which is restored to its full amplitude by the integrators. Because of nonlinear opamp gain and slew-rate effects, harmonic components of the input signal are created at the outputs of the integrators, in y_{11} and y_{12} , and will appear at the output of the modulator in v , shaped by first- and second-order highpass transfer functions, respectively. The attenuation provided is satisfactory if a high oversampling ratio is used. For example, if $OSR = 128$, harmonics in y_{11} are reduced by at least 32.2 dB. However, if $OSR = 8$, the attenuation is only 8.2 dB. In wideband applications, where high-speed analogue processing blocks are required, designing a sufficiently low distortion opamp to deal with this problem can be impractical.

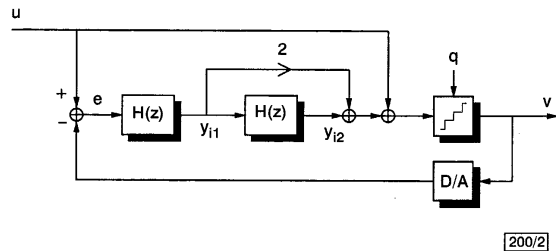


Fig. 2 Proposed reduced distortion topology

Proposed topology: The nonlinearity problem can be solved by cancelling the transfer functions from u to y_{11} and y_{12} . This is achieved by making $STF(z) = 1$.

One possible implementation is shown in Fig. 2 [1, 2]. The noise transfer function is unaffected, but the integrators will now process quantisation noise only. Therefore, their performance requirements can be significantly relaxed. Another advantage is that only one DAC is required in the feedback loop. For multibit quantisation, this reduces the circuit complexity and chip area significantly.