

# Optimal Supply Voltage Selection through a Multiobjective Design Strategy

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## Abstract

*Power consumption has become an increasingly important VLSI parameter in recent years primarily due to increased clock frequencies and integration. The advent of System-on-Chip design, utilising ULSI scales of integration, increases the requirement for high-level CAD tools capable of power reduction. This paper presents a stochastic, multiobjective CAD tool that synthesises low-voltage signal-processing systems. The multiobjective nature of the tool enables a range of low-voltage systems to be synthesised, permitting the selection of the system that best meets the global requirements of the System-on-Chip. Results are presented which illustrate the design information created for typical signal processing algorithms.*

*Conference Keywords – Analog & Digital VLSI Signal Processing, DSP Hardware & Software, Application-specific circuit/processor design*

## I. INTRODUCTION

In recent years the power consumption of VLSI devices has been identified as of major concern alongside the traditional objectives of min-area and max-speed [1,2,3,4]. This has led to the development of a number of power optimisation strategies that consider power at all levels of the VLSI design process [5,6,7,8]. Previous research has shown that early intervention through consideration of power consumption at the high-levels of the design process yields the most significant power reductions [9,10,11,12].

A notable technique for high-level power reduction has centred on the synthesis of low-power Digital Signal Processing (DSP) ASIC devices [13,7,14]. These are of particular importance due to their complexity and high speed. The technique has been incorporated into various

CAD tools, with power reductions of an order of magnitude reported [7,15]. The technique manipulates high-level behavioural descriptions of DSP algorithms, to synthesise low-voltage, minimum-area devices with no impact on the computational throughput. Utilising this high-level technique, DSP devices with a required throughput are modified to accept low-voltage operation without the resulting speed decrease inherent in reducing the supply voltage of CMOS devices [13,7].

The high-level power-reduction technique produces DSP systems that require specific voltages to obtain the lowest possible power consumption. This has implications when incorporating the specialised-voltage devices in other systems, especially in the case of complex System-On-Chip (SOC) design [16,17]. SOC system implementation has become increasingly feasible in recent years as the complexity of VLSI devices has increased. Such systems typically contain a number of key components, or 'cores', each of which needs to be optimised in terms of power, area and speed parameters to produce a globally optimised system. Combining separately optimised cores on the same chip, each with specific supply-voltages to meet optimal area, speed and power requirements, requires the use of on-chip voltage level converters [18,19]. These converters add to the amount of circuitry required in the system, increasing the overall area and power consumption, reducing the benefits obtained with the low-voltage optimisation process.

Defining a global supply voltage for the system can eliminate this requirement for additional level conversion circuitry. However, the high-level optimisation tools, producing a single lowest voltage solution, may produce cores that are incompatible with the global voltage and may also require prohibitive implementation area. To contend with this problem, this paper presents a multiobjective CAD tool that presents a family of low-voltage and minimal area solutions to enable the selection of the design that best meets the system requirements while still producing low-power solutions. The paper

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proposes a methodology for analysing the design information provided by the tool in selecting the optimum supply voltage.

## II. IMPLEMENTATION

The paper presents a CAD tool which optimises DSP algorithms from the high-level of abstraction, thus producing significant supply voltage reductions. The technique is based on a heuristic search mechanism developed for low-voltage design synthesis [20]. The system incorporates an application-specific (hybrid) genetic algorithm (GA) [21]. GAs are an increasingly popular technique for the solution of problems that present a complex set of multi-objective tradeoffs. The GA performs a parallel search of the solution space to determine the optimum core design. During the optimisation process the GA evaluates many alternative solutions. The information obtained from these evaluations is used to create a family of solutions for that core algorithm with different implementation requirements. Rather than present a single lowest-voltage solution, the CAD tool discussed in this paper uses multiobjective GA (MOGA) search techniques to present a family of solutions to the SOC VLSI designer. Each solution corresponds to a minimum area implementation of the DSP algorithm, with no loss in throughput, for a particular supply voltage.

The operation of the core optimisation system is illustrated in figure 1. The system processes algorithms described as Data Flow Graphs (DFG). The DFG forms a design seed that initializes the stochastic process by creating a number of designs, with different performance specifications, through the application of one or more transformations. These are selected from a *transformation set* which includes the following:

1. Retiming
2. Pipelining
3. Loop Unfolding
4. Automatic Pipelining

The stochastic search applies the high-level exploration techniques to generate a set of Pareto-optimal designs. These techniques are genetic algorithm operations (such as mutation and crossover) specifically modified to incorporate the high-level transformations.

A key feature of the optimisation system is its parallel search technique, evaluating many designs throughout the search process. Modification of the standard GA search

technique enables collection of a set of 'non-dominated solutions' from this parallel search.

The original specification is translated (T) into a DFG representation before submission to the stochastic search technique. The stochastic search applies the high-level exploration techniques to generate a family of optimal solutions.

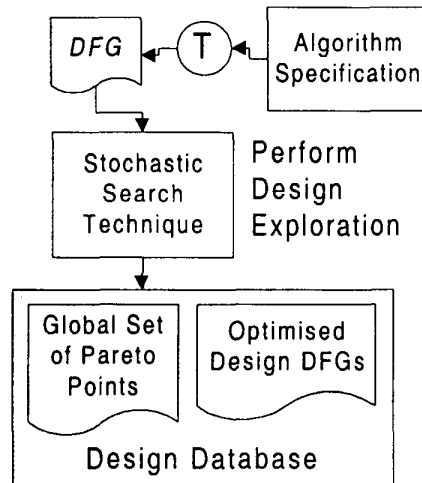
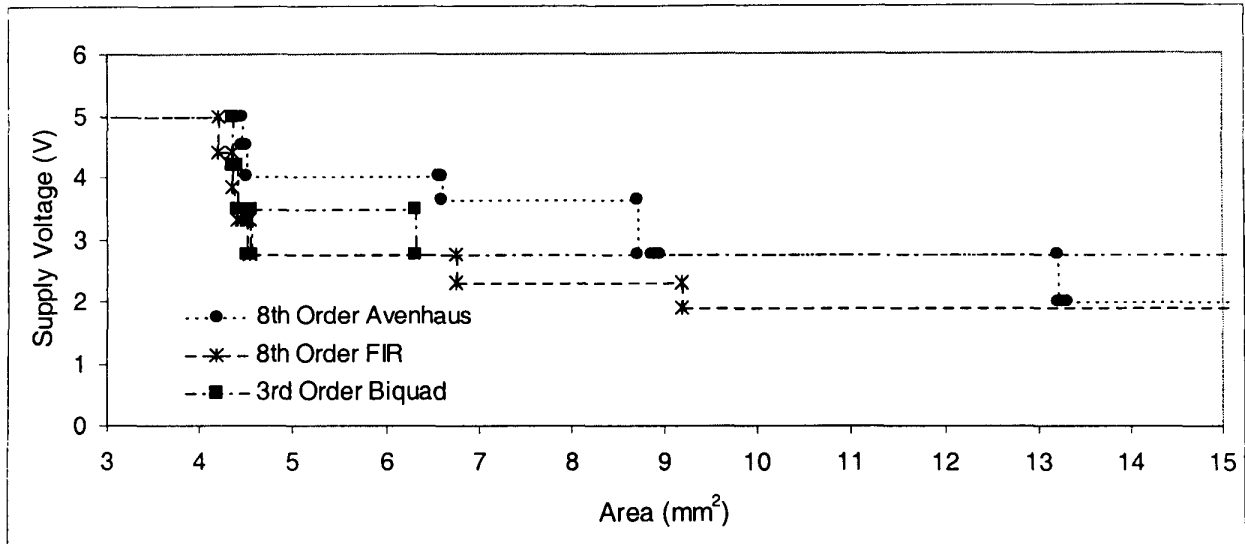


Figure 1. Core Optimisation System

The family of solutions is presented to the designer as a *design database*; this comprises the set of optimised designs and the voltage-area tradeoff analysis, presented as a Pareto-surface [21]. This design database enables the designer to select the design that best meets the system implementation requirements, such as the solution that conforms to the global voltage for the entire system.

The Pareto-surface information also assists the designer in making global SOC design decisions; for example, the information may indicate that a small reduction in the global voltage may enable a considerable power reduction in the DSP core. The design database also provides information for assistance during floorplanning as each low-voltage solution is a minimum area implementation at that voltage. The design information may indicate that a slight increase in the floorplan area allocated to the core will enable a lower-voltage solution to be used.

The methodology for selecting the optimal solution must consider the global constraints of supply voltage and area. One technique is to drive the supply voltage as low as



**Figure 2.** Design trade off with a number of benchmark examples

possible by selecting the minimum voltage. Tolerances on area and power can then be used to move through the design database to determine the best solution. For example, if the lowest voltage solution has another solution within +10% of its supply voltage, but with a >10% reduction in area, then the higher voltage solution is selected where the >10% area saving is regarded as desirable. This process is executed for the system cores to arrive at a global supply voltage with minimum area implementation. In effect, the global solution for selection is another multiobjective problem which is solved for each system using the VLSI designers expert knowledge.

## I. RESULTS

The systems analysed in this paper are all assumed to have a nominal supply voltage of 5V. However, the power reducing techniques are also applicable to systems with a lower nominal supply voltage. Figure 2 illustrates the Pareto-surface information obtained for typical DSP algorithms; an 8<sup>th</sup> order Avenhaus filter, and 8<sup>th</sup> order FIR filter and a 3<sup>rd</sup> order Bi-quadratic filter structure. A straight line is used to represent the pareto-surface (the boundary between feasible and infeasible solutions) due to the nature of the VLSI synthesis problem; solutions exist at discrete points in the solution space. A curve may imply that there is a range of solutions with different voltage and area characteristics available between each point. The

advantages of the design database can be illustrated by examining the 8<sup>th</sup> order Avenhaus results. The information illustrates that the lowest voltage design (1.9V) has an area of approximately 13mm<sup>2</sup>; however, a design with a voltage of 2.75V has an area of 8.7mm<sup>2</sup>. A far smaller design can be used, to reduce the area requirements of the entire system, while still obtaining power reductions through the use of a low supply voltage. The constraints of the global system can be used to select the best design that meets the implementation requirements.

The Global SOC design may require all of these DSP cores – the design information illustrates all possible minimum area with minimum voltage implementations. This information could be used to select a global minimum supply voltage (2.7V as all designs have a solution at this voltage) and analyse the effect on area or this information can be passed to a second stage optimisation system to determine the best overall tradeoff between supply voltage and area.

## II. CONCLUSIONS

This paper has presented a CAD tool for the efficient selection of low-voltage components for complex SOC system implementation. The CAD tool enables the system designer to optimise the individual components for minimum area and power consumption while maintaining

the area, power and supply voltage constraints of the system.

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