

# LOW POWER DOMAIN-SPECIFIC RECONFIGURABLE ARRAY FOR DISCRETE WAVELET TRANSFORMS TARGETING MULTIMEDIA APPLICATIONS

Sajid Baloch<sup>1,2</sup>, Imran Ahmed<sup>1,2</sup>

Tughrul Arslan<sup>1,2</sup>, Adrian Stoica<sup>2,3</sup>

1: Institute for System Level Integration, The Alba Centre, The Alba Campus, Livingston, EH54 7EG, UK

2: School of Electronics & Engineering University of Edinburgh, Kings Buildings, Mayfield Road, Edinburgh EH9 3JL UK

3: NASA, Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, CA 91109, USA

## ABSTRACT

Domain-specific heterogeneous reconfigurable arrays provide high performance over generic Field Programmable Gate Arrays (FPGAs) while maintaining the flexibility for that particular domain. This paper introduces an embedded domain-specific reconfigurable array that targets discrete wavelet transforms (DWT) and also presents different configurations of the array to prove its suitability for complex algorithms which are part of changing standards like JPEG and MPEG etc. The proposed array is flexible in order to accommodate various 5/3 and 9/7 discrete wavelet transforms which makes it quite suitable for multimedia applications. Experimental results demonstrate that the proposed architecture is over 31% more efficient in terms of power consumption over standard FPGAs.

## 1. INTRODUCTION

The demand for image/video applications in portable form has greatly increased in recent years. At the core of these productive and useful applications is image/video compression technology. The DWT is one of these algorithms and technologies that had been developed for the compression of digital image/video data. The DWT is becoming popular because of the fact that it has features such as progressive image transmission by quality/resolution and it provides an easy way to manipulate compressed images. Such features lead to significant interest in producing efficient algorithms for the realization of DWT hardware, for example, convolution based DWT, lifting based DWT and integer DWT etc. Each has its own merits and demerits and which make them suitable for different multimedia application.

Current reconfigurable logic and Field Programmable Gate Array (FPGAs) provide quite powerful, flexible and cost-effective solutions for broad range of applications. The emerging trend in reconfigurable logic is Embedded Reconfigurable Arrays (RA). These RAs could benefit from parallel executions. Several companies [1][2] have introduced commercial embedded FPGAs. Embedded

Reconfigurable Array in System-on-Chip (SoC) can provide extra flexibility to the ASIC. This flexibility helps to accommodate post-fabrication modifications and also helps in reducing development time, debugging of errors, reduction in time-to-market and to add new functionality without going again into design stage. These all factors contribute in, reducing the overall cost of the product. Such flexibility is very useful for implementing complex algorithms which are part of changing standards like JPEG etc.

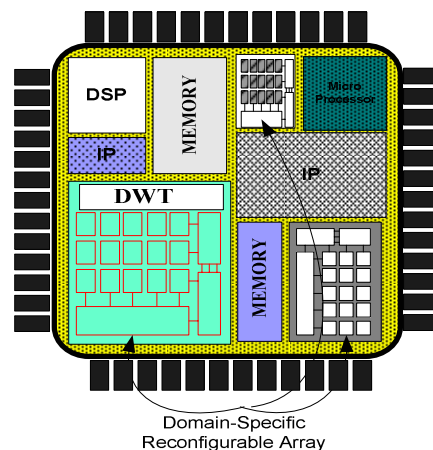


Fig-1: Basic Theme of SoC with reconfigurable arrays, each targeting a specific domain of computations.

This paper presents a domain-specific RA targeting Discrete Wavelet Transform (DWT). The RA proposed is flexible enough to accommodate various DWT algorithms, while maintaining high performance in terms of area and power consumption. There has been no reconfigurable architecture proposed so far in the literature, which can incorporate the calculation of 5/3 and 9/7 DWT based upon Lifting based, Classical (convolution) based and integer based DWT algorithms. The proposed reconfigurable architecture is unique as it can perform both 5/3 and 9/3 DWT calculations based upon the afore said algorithms while maintaining the flexibility of RA and making the architecture power efficient over the FPGAs at the same time.

The authors have already introduced an array for DCT computations for hand-held devices [3]. The presented array permits a low-power and high throughput solution for complex calculations like DWT as it is more optimized in terms of interconnects than the previously introduced DCT array. At the same time it provides flexibility to allow changes to be accommodated after fabrications, hence, it represents a compromise between FPGAs and hardwired implementation in terms of flexibility, power consumption and area.

## 2. DIFFERENT BLOCKS OF R.A.

A simple DWT implementation on the proposed RA requires adder, subtractor, multiplier and divider blocks. In order to accommodate a wide range of DWT algorithms, elements such as ‘programmable buffers’ and ‘programmable normalizing blocks’ are also required. MATLAB simulations were performed to figure out the minimum bit width for lossless and lossy image processing for our architecture. It was decided on the basis of the simulation results that minimum 16-bits are required for 5/3 DWT and 20-bits for 9/7 lifting based DWT (sign bit included) are required to conform with JPEG standard. The proposed array has three type of blocks/elements. These elements are described below;

### 2.1 Add-subtract Cluster

The add-subtract cluster can be configured as:

- parallel, digit-serial or bit-serial adder/subtractor
- can perform A-B and B-A operation

The basic module is 8-bits wide, three modules are grouped into cluster and configurable switches are provided between them to support cascading to get wider bit ranges (up to 24-bits). Even wider bit ranges are possible for different operations by cascading multiple clusters through mesh interconnect. The different configurations of Add-subtract cluster can be selected through configuration bits reserved for the cluster. The precision of the calculation can be selected by configuring the cluster depending upon how many modules are required ( basic module is 8-bits wide). 16 bits are required for the loss-less calculation based upon 5/3 which can be achieved by incorporating two basic modules through configuration switches. Flexibility of selecting the bit-widths, makes the architecture more versatile.

### 2.2 Coefficient Multiplier Cluster

Filter coefficients are multiplied through configurable coefficient multiplier clusters. Hardwired multipliers always give better performance in terms of power over the real multipliers. The cluster performs multiplication by carrying out a number of shift and addition operations. The floating point coefficients (for 9/7 lifting based DWT) are implemented through canonical-

signed-digit (CSD) form [4]. The cluster has programmable shifter blocks, adder blocks and a multiplexer to accommodate a wide range of coefficients. The cluster can handle up to 24-bit operation to facilitate required precision. Filter coefficients for 9/7 lifting based DWT are incorporated through CSD and explained through the table-1.

	Value	12-Bit CSD Representation
Alpha	1.586134342	$2^1 \cdot 2^{-1} + 2^{-3} \cdot 2^{-5} \cdot 2^{-7} + 2^{-12}$ =1.5861816
Beta	0.052980118	$2^{-4} \cdot 2^{-7} \cdot 2^{-9} + 2^{-12}$ = 0.0529785
Gamma	0.882911076	$2^0 \cdot 2^{-3} + 2^{-7} = 0.8828125$
Delta	0.443506852	$2^{-1} \cdot 2^{-4} + 2^{-7} \cdot 2^{-9} + 2^{-12}$ =0.4436035

Table-1 9/7 Filter coefficients in CSD form

The cluster is shown below:

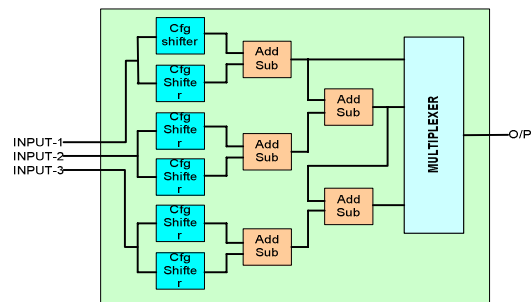


Fig-2 shows the internal structure of the coefficient multiplier cluster. The cluster has three internal sub-module.

- Cfg-Shifter Module
- add-Sub Module
- Multiplexer Module

Cfg-Shifter performs the multiplication and division depending upon the algorithm. It can be configured to multiply or divide by any even integer value between 2 and 32. add-sub is the same as explained in section 3.1. The multiplexer is configured to select one of its inputs based upon the DWT algorithm. All internal modules are interconnected through programmable switches to incorporate different multiplications and divisions.

### 2.3 Configurable Buffer Cluster

The cluster can be programmed in 4-bit, 8-bit, 12-bit, 16-bit, 20-bit and 24-bit different combinations. A wider bit-range of operations can be handled by incorporating multiple clusters with the help of an interconnect mesh. The cluster can be used as buffer/delay element towards the hardware realization of a DWT algorithm. The cluster

also provides configurable normalizing functionality depending upon the DWT filter type i-e 9/7.

### 3. ARRAY FOR DWT

The uniformly arranged clusters in columns make it simpler to make manual routing and placement while configuring the array. The arrangement of the clusters in the array is done at the design-time and according to the application and required flexibility. The array is organized as shown in Fig-3. The elements of the array are interconnected through symmetrical configurable switches. Twenty four 4-bit tracks and twenty four-1bit tracks are provided for both data and control lines. Connection boxes (C-Boxes) connect the pins of the cluster to the tracks, and the switch boxes (S-Boxes) connect together the intersection of the tracks [6].

The C-boxes has flexibility  $F_c=24$  and S-Boxes with  $F_s=3$  [6]. Values selected for simplicity and sufficient flexibility to incorporate different algorithms of DWT. Different values can be selected by the designer depending upon the application requirements. Tri-state buffers are used for configurable switches. The connection of clusters with tracks is illustrated in Fig-4.

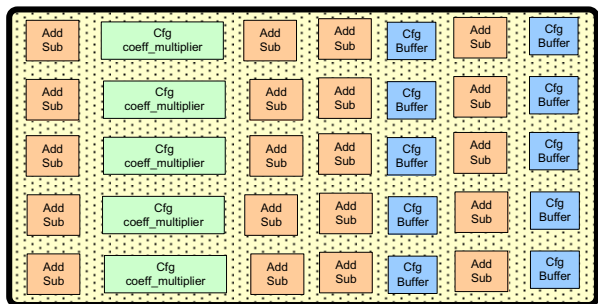


Fig-3 Arrangement of the clusters in the RA

The decision to use tri-state buffers over pass transistors is inspired by the fact that the tri-state buffers make the architecture to fit easily with the design flow used for the rest of the SoC and is more customizable at the design-time.

#### 3.1 DWT Implementation-1

An efficient implementation method of DWT [7] and its hardware realization DWT in terms of our proposed array is shown in Fig-7. The implementation is efficient and quite unique as it requires a few numbers of elements as compared to [5]. The implementation takes three inputs in a fashion shown in the Fig-6. The implementation [7] has 100% reusability in terms of implementing 5/3 and 9/7 lifting based DWT. The proposed implementation uses only one buffer and gives output/DWT coefficients on every clock cycle while [5] requires 6 pipeline and 4

pipeline registers and initially requires more than one clock cycle to give the first output. This hardware realization as shown in Fig-6, was used to bench mark performance of our proposed array against standard FPGAs. 5/3 and 9/7 lifting based DWT algorithms were implemented on this architecture. These are explained as below.

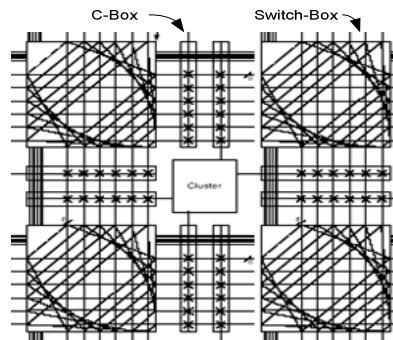


Fig-4 Basic mesh interconnect scheme

5/3 lifting based DWT has many advantages over other DWT algorithms such as, the 5/3 helps to achieve lossless image compression and 5/3 has short filter length for both low-pass and high-pass filter as compare to other JPEG2000 specified DWT filters i-e Daubechies 9/7 filter. 5/3 Filter has only one set of lifting step compared to 9/7, Which has two.

The implementation of 9/7 lifting based is carried out through the same architecture as shown in figure-4. The important feature of this implementation is that the configuration for the RA is same for the 5/3 and 9/7 lifting based DWT. This allows the array to be dynamically reconfigured for both 5/3 and 9/7. The multiplier block is re-configured to incorporate the 9/7 lifting based ‘predict’ and ‘update’ coefficients. The coefficients of filters are implemented on the basis of canonic-signed-digit (CSD) form [4] as explained in previous section.

#### 3.2 DWT Implementation-2

Lian et al. have proposed an architecture for the implementation of 5/3 and 9/7 lifting based DWT[5].

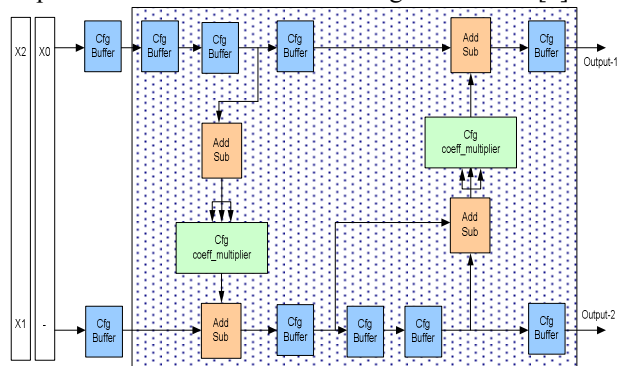


Fig-8 Realization of Lian Architecture[5] in terms of proposed Reconfigurable Array  
Hardware realization of Lian’s architecture in terms of our

RA is shown in Fig-8. The same hardware is used to implement 5/3 and 9/7 lifting based DWT. The reconfigurable blocks of array (explained earlier) were configured to implement 5/3 lifting based DWT. The hardware realization of Lian et al architecture (Fig-8) was again used to implement 9/7 lifting based DWT and all blocks/elements of RA were configured accordingly. The results were analyzed to bench mark our RA (explained later).

#### 4. PERFORMANCE EVALUATION

Hardware realizations of two different DWT architectures were carried out on the proposed array to evaluate its performance. 5/3 and 9/7 lifting based computations were performed on each hardware realization as explained earlier to show the suitability of our proposed array for a specific domain of applications (lifting based DWT). The same algorithms were implemented on different architectures (Standard FPGA) and were compared. The performance results are discussed below: The performance in terms of overall power consumption and maximum operating frequency is shown in Table-2 and Table-2. All these systems use 0.18 $\mu$ m CMOS technology and run at 1.8V. The values are measured for single frame of a 128x128 Lenna image.

DWT Architecture [7] Implemented on	Power Consumption (mw)	Max Frequency (MHz)
<b>Xilinx Virtex-E</b>		
5/3 lifting based DWT	9.98	98
9/7 lifting based DWT	12.48	73
<b>Proposed RA</b>		
5/3 lifting based DWT	6.13	123
9/7 lifting based DWT	12.48	123

Table-2 Performance Evaluation of Proposed Array  
The Hardware realization of Lian et al. DWT architecture [5] (explained in section 4.2) was used to obtain the following results in table 4..

Lian DWT Architecture [5] Implemented on	Power Consumption (mw)	Max Frequency (MHz)
<b>Xilinx Virtex-E</b>		
5/3 lifting based DWT	23.10	83
9/7 lifting based DWT	40.68	66
<b>Proposed RA</b>		
5/3 lifting based DWT	14.87	110
9/7 lifting based DWT	26.90	110

Table-4 Performance Evaluation of Proposed Array (Lian et al DWT Architecture [5])

The values provided include the power consumed by the configuration circuit and configuration memory. Our proposed array consumes between 31% and 38% less power than the Virtex-E. This is mainly caused by the fact

that less interconnects and larger clusters are used in our array.

Our array has a maximum frequency 21% to 40% higher than the Virtex-E, however it is still 45% to 56% less than the maximum frequency achievable in ASIC. The reduced frequency is understandable as it is because of the delays introduced due to reconfigurable switches.

#### 5. CONCLUSION

In this paper, we present a domain specific reconfigurable array architecture. The elements within the proposed array are arranged with a mesh of reconfigurable interconnects. The re-configurability of the array permits mapping a number of distributed arithmetic implementations such as DWT and filtering calculations used in video coding. Two DWT calculations were implemented on the RA. These were also implemented in a standard commercial FPGA. It was demonstrated that the array provides approximately 31 to 38% reduction in power consumption over FPGA and an improvement of about 20 to 40% in timing. These figures show that the proposed array architectures provides a good compromise between hardwired ASICs and generic FPGAs in terms of flexibility, area, timing and power consumption when targeting a domain-specific application.

#### 6. REFERENCES:

- [1] S.Baloch, S.Khawam, T.Arslan, I.Ahmad, A.Kasturi, Efficient Implementations of Mobile Video Computations on Domain-Specific Reconfigurable Arrays. DATE Conference and Exhibition, 2004.Proceedings Volume 2, 16-20 Feb. 2004
- [2] Bryant I., Tanurhan Y., "The Actel Embeddable FPGA Core", Actel Corporation, 2001
- [3] eASIC, "eASIC 0.13um Core", www.easic.com
- [4] K. Andra, C. Chakrabarti and T Acharya, "A vlsi architecture for lifting based forward and inverse wavelet transforms", IEEE transaction on signal processing, Vol. 50, Issue 4, April 2002 Page(s):966 - 977
- [5] C-J Lian, K-F Chen, H-H Chen and L-G Chen, Lifting based discrete wavelet transform architecture for JPEG-2000, Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on Volume 2, 6-9 May 2001 Page(s):445 - 448 vol. 2
- [6] Rose J., Brown S., "Flexibility of interconnection structures for field-programmable gate arrays", Solid-State Circuits, IEEE , Vol.26, Iss.3, 1990, Pgs: 277- 282
- [7] SBaloch, T. Arslan, Domain-Specific Reconfigurable Array Targeting Discrete Wavelet Transform for System-on-Chip Applications, Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International 04-08 April 2005 Page(s):161a - 161a