

# Design of a Single Event Upset (SEU) Mitigation Technique for Programmable Devices

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## Abstract

*This paper presents a unique SEU (single Event Upset) mitigation technique based upon Temporal Data Sampling for synchronous circuits and configuration bit storage for programmable devices. The design technique addresses both conventional static SEUs and SETs (Single Event Transients) induced errors that can result in data loss for reconfigurable architectures. The proposed scheme not only eliminates all SEUs and SETs and but also all double event upsets as well. This approach permits FPGAs and other microcircuits with deep submicron feature size to be used in space environments. The result are included to show that the proposed scheme is over 40% area efficient than previously introduced schemes.*

## 1. Introduction

Single event upset (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." [1]. SEUs are soft errors, and are nondestructive. An SEU may occur in analogue, digital, optical components, or may have effects in surrounding interface circuitry.

Programmable Logic Devices, and more specifically Field Programmable Gate Arrays (FPGA), are replacing traditional logic circuits by offering the advantages of high integration (small size, low power, and high reliability) without the disadvantages of custom ASICs (high nonrecurring engineering cost and high risk, especially in limited production volume). FPGAs based on SRAM technology offer an additional unprecedented advantage. These can be reprogrammed an unlimited number of times, even in the end-user system. In these FPGAs, a multitude of latches, also called memory cells or RAM bits, define all logic functions and on-chip interconnects. Such latches are similar to the 6-

transistor storage cells used in SRAMs, which has proved to be sensitive to single event upsets caused by high-energy neutrons [7]. The faults have been observed as bit errors in memories. The phenomenon has been observed at both aircraft altitudes and on ground [2][3][4], and is now considered an issue in the dependability of airborne electronics [2].

As the microelectronics industry has advanced, Integrated Circuit (IC) design in general and reconfigurable architectures (FPGAs, reconfigurable SoC and etc) in particular have experienced dramatic increase in density and speed due to decrease in feature sizes with which these devices are manufactured. The effects of scaling on the single event response of microelectronics are a direct result of the physics of energy loss, charge collection, and upset due to a cosmic ray striking a junction in an IC device. The review here is brief and qualitative. Many good summaries exist [5], [6], [7] that review these concepts in more detail.

When an energetic ion passes through any material it loses energy through interactions with the bound electrons, causing an ionization of the material and the formation of a dense track of electron-hole pairs. The rate at which the ion loses energy is the stopping power ( $dE/dx$ ). The incremental energy  $dE$  is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units of  $mg/cm^2$ . The radiation effects community has adopted the term LET (Linear Energy Transfer) for the stopping power. An ion with an LET of  $100 MeV\text{-}cm^2/mg$  deposits approximately  $1pC$  of electron-hole pairs along each micron of its track through silicon.

In the presence of electric fields, these electron-hole pairs quickly separate as they drift in opposite directions in the field and are quickly collected by whatever voltage sources are responsible for the field, thus producing a current transient. In bulk CMOS designs, such electric fields are present across every 'pn' junction in the device. If an ion strikes a junction connected to a signal node, a current transient is subsequently observed on the signal node as the electric fields in the junction and funnel regions separate the electron and hole carriers. The initial prompt current pulse is short lived, lasting on the order of only 100 to 200 picoseconds.

High energy protons and neutrons are also known to produce similar effects indirectly through nuclear reactions within the silicon. In these cases, a heavy ion recoil reaction by-product passes through a junction and produces a similar charge collection current pulse. In space, high energy protons primarily originate from the trapped proton radiation belts and from solar flares. For high-altitude aircraft, both high energy neutrons and protons are encountered as reaction by-products found in cosmic ray showers formed when an energetic heavy ion from space undergoes a nuclear reaction in the atmosphere. These induced currents are responsible for SEUs observed in space-borne circuits, typically static latches and SRAMs (Static Random Access Memories), over the last 10-15 years [4]. The effect that these currents have on a circuit depends on the response of the circuit to the charge collected on the signal node. Basically, the capacitance of the signal node (to first order) determines how large a voltage swing  $dV$  results from the collection of a charge  $dQ$  according to  $dV=dQ/C$ . For latches and SRAMs, positive gain feedback loops result into a data bit flip once the collected charge reaches a critical value sufficient to drive a node voltage past the switching voltage.

## 2. UPSET MECHANISM

SEU in static latches and SRAMs became an important issue once feature sizes dropped below 10 microns and the critical charge for upsetting a circuit dropped below 1 pC (roughly corresponding to a particle LET of 50MeV cm<sup>2</sup>/mg and a collection depth of 2 microns). Static latch SEU vulnerability has been calculated [3] and measured [6] as a function of technology feature size to establish the relationship between the critical charge, needed to upset the circuit and the technology feature size. All results indicate that the critical charge needed to upset a latch decreases as the square of the feature size. If this relation holds as electronics feature sizes decrease from 0.8 micron (spaceborne architectures) to 0.18 micron, the critical charge decreases by nearly a factor of 20.

The FPGA's configuration bits (Bit-stream) are used to configure both the logic elements and the routing switches. Upset of a programming bit in a FPGA is much more serious than a conventional data bit upset. If a logic element control bit changes state, then the logic functionality of the FPGA is altered. If a control-bit of routing switch experiences an upset, then the FPGA essentially becomes rewired. In either case, the programmed circuit function is no longer what was intended. For these reasons, the configuration storage of the FPGA must be totally immune to SEU.

In this work, we propose a novel design technique to cope with both SEU and SET faults. The design technique is based upon unique temporal data sampling. In comparison to the work done so far on temporal sampling [8][9][11], the proposed technique needs only three clock signals rather than four. Saving of a clock signal, results in low area and power cost. Design complexity can always be attributed with the total number of components required. Total number of

latches required to implement the proposed technique is 40% to 51% less than the previously introduced architectures [8][9][11], hence, proposed design is far more simpler. As shown by the simulation results, the proposed design is area efficient due to reduced number of latches for data sampling. The proposed voting circuitry considers logic state of every node of the circuit to evaluate an SEU free output. Unlike the previously proposed schemes [8][9][11]. Due to combination of temporal sampling and majority voting, the proposed design gives 100% fault recovery from SEU and SET, along with 100% fault recovery from dual event faults.

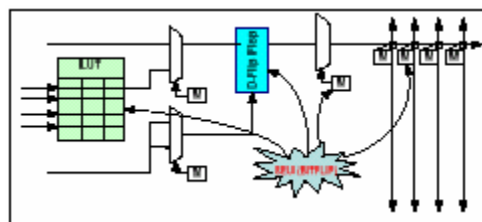


Figure 1: SEU Sensitive Configuration Bit Storage Circuit

If a heavy ion strike occurs within the combinatorial logic block of a sequential circuit, and the logic is fast enough to propagate the induced transient, then the SET will eventually appear at the input of a data latch where it may be interpreted as a valid signal. Similar invalid transient data might appear at the outputs of lookup tables (LUTs) and on routing lines due to SETs generated in the programming elements, particularly for the case of EEPROM storage elements (Figure-1). Whether or not the resulting SET gets stored as real data depends on the temporal relationship between its arrival time and the falling edge of the clock. Similarly, SETs on clock, reset, and control lines can result in the storage of incorrect data within the data latches.

Nonvolatile, reprogrammable FPGAs typically use EEPROM transistors to store the configuration data. The programmed threshold voltage of a EEPROM transistor is simply not large enough to provide charge dissipation drives comparable to normal CMOS transistors. It results in relatively wide SETs that propagate in FPGAs which are fabricated in technologies having feature sizes as large as 0.8 micron. The SET induced error rates in these cases can actually exceed SEU rates at frequencies of only a few tens of MHz [10].

## 3. TEMPORAL DATA SAMPLING

The first key step in our newly proposed technique is 'Temporal Data Sampling'. A simple embodiment of the Temporal Data Sampling is shown in the Figure-2. The circuit consists of five 'edge-sensitive flip-flops' as shown in Figure-2. Each flip-flop operates in 'Sampling Mode' when its respective clock signal is in high state and in 'Blocking Mode' when clock signal is low. In 'Blocking Mode' flip-flop holds the data and data changes are blocked. In sampling mode the flip-flop behaves 'transparent' to the incoming data.

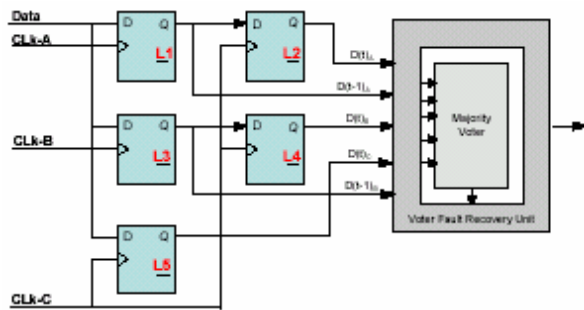


Figure 2: Proposed Temporal Data Sampling

The Temporal Sampling stage helps to store Data samples at different time intervals. These samples are used in voting logic to eliminate single event upsets. Three different clocks (Clk-A, Clk-B & Clk-C) are used. These three clocks are derivative of the main clock and have a 90-degree phase shift and 25% duty cycle to cope with the SETs as shown in Figure-2. If SEU is observed on any one of the clock lines, the phase shift in the remaining clock signals will help the respective set of flip-flops to store the correct data at different time intervals, hence voiding the effect of spurious glitch on the clock line due to radiation. Any transients due to radiation last for small period of time and if it happens at the negative edge of any clock signal, it will die out before the other temporal flip-flop start their operation due to phase-shift in clock signals. Therefore, this clocking scheme will help to cope with all the single event transients either in Data line or any one of the clock signals. A conventional (SEU susceptible) sequential circuit would satisfy timing constraints such that the maximum combinatorial logic transition time would be less than the period of the master clock minus setup time for the D-Flip-Flop. In our proposed technique, data is released on the edge of CLK-C, and must reach the next sampling stage before the edge of CLKA (minus the setup time).

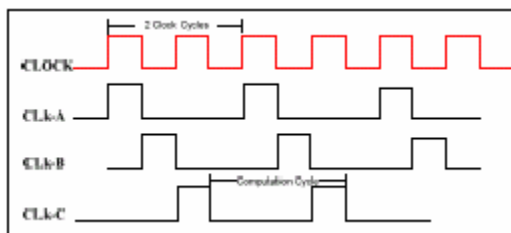


Figure 3: Clocking Scheme for the proposed Architecture

The insertion of the two extra clock phases (CLKB and CLK-C) is required for the additional temporal sampling. Figure-3 illustrates the clocking scheme. The effective, on-chip computational frequency is exactly one half the frequency of the master clock. Therefore speed penalty by a factor of two has been incurred to ensure complete upset immunity.

The proposed design technique has two stages, data sampling and data release stage. Flip-flops L1, L3 and L5 constitute the data sampling stage while L2, L4 and L5

constitute Data release stage of the proposed technique. Flip-flop L5 is common in both stages. The sampling stage FFs capture data at different time intervals based on their respective clock signals. Clock-C serves as sampling clock as well as sample release clock. For any given data, two samples of data are stored at different time intervals (Clk-A, Clk-B). Third data sample is stored at time  $t$  (Clk-C) and at the same time previously stored samples are released to majority voting logic along with this data sample.

Lima, F. et al.[11] proposed an architecture which is based upon 'dice cell'. The scheme uses 4 clock signals to take samples in contrast to our proposed scheme which takes only three. The reference scheme uses 9 memory elements and gives Single event Upset/Transient immunity while our proposed scheme uses less memory elements (only 4 memory elements) and immune to all SEU/SET and double event faults as well. One might expect the temporal sampling flip-flop to occupy 4-times more IC area than conventional D-Flip-Flop based techniques (TMR, etc). For any given ASIC design, however, the total chip area will never grow by a factor of five. This can be explained as below. All of the combinatorial logic can remain unchanged and only the D-Flip-Flops in the design must grow. The amount that any given ASIC must grow will depend on the ratio of D-Flip-Flop area to total chip area for example fan anti-jam filter, has 7.5% of its area devoted to D-Flip-Flops [7] and an 8-bit ALU, contains addition, subtraction, bit shift, and bit logic blocks. The fraction of this chip devoted to D-Flip-Flops is only 7.2% [7]. The total size penalty, expressed as an area increase factor, for using temporal sampling latches in these chips would therefore depend on the number of latches only.

#### 4. MAJORITY VOTING

Majority voting is commonly used in TMR systems. The proposed mitigation technique is based upon simple majority voting. All the data samples which were stored at different time intervals are fed into majority voter circuitry. The data samples from 'sample release stage' are compared with each other. Data is considered 'Fault Free' if no disagreement is found. On the other hand, if disagreement is found, the data samples from the 'sampling stage' are considered to evaluate Fault Free output. The samples from the 'sampling stage' provide more data value to compare and evaluate fault free value. This unique feature helps to eliminate all SEUs and SETs and as a unique feature rectifies all Double Faults (DF) as well.

The majority voting circuitry is equipped with a watchdog circuit with checks for the voter faults. This is one extra level of security on the voter calculations. In case of voter circuit faults the over-ride functionality corrects the output.

#### 5. EXPERIMENTAL FLOW

The proposed technique is coded in 'C' program, which takes net-list of the circuit under test as input. D-flip-flops are identified and structural modifications are made to the original circuit. The modified net-list is then fed into

software simulator to analyse the behaviour of the circuit under SEUs/SETs. The net-list is can be mapped on any reconfigurable architecture (FPGA etc) through a suitable software tool (Xilinx Foundation Tool etc).

## 6. RESULTS

The Experimental results are derived for a medium sized circuit ISCAS89 benchmark circuits S386 contains 12 Flip-Flops. We injected 100 random SEU, SET faults, double event upsets (DEU) and triple-event upsets (TEU) to verify our proposed scheme. Faults were injected through software simulations. Ref [11] has the limitation that scrubbing is required before the second fault occurs which limits the overall system performance. The proposed scheme can handle all the double faults which can reduce the scrubbing frequency to half and enhances the system performance.

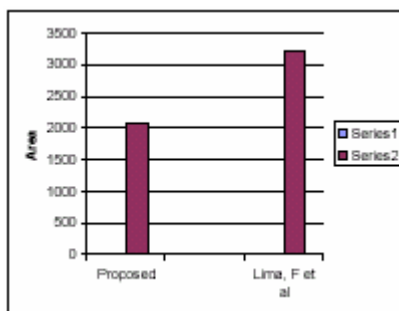


Figure 4: Area Comparison

There was no area or power analysis done for previous architecture to compare with the proposed scheme. So authors implemented proposed technique and Lima, F. et al technique on 0.13 um CMOS technology. Figure-4 illustrates the area calculation. Area saving of 51% is achieved for the circuit under test. Figure-5 shows 48.6% Power saving through proposed technique.

The result clearly shows that our proposed scheme is much more efficient than other techniques. The scheme not only gives 100% fault recovery from all single event faults but also from double event faults.

## 8. CONCLUSION

This paper has described a new concurrent SEU/SET mitigation technique for reconfigurable architectures. The proposed scheme gives immunity against all single faults and double faults as well with auto correction mechanism. Due to this added feature, scrubbing is no longer required. The proposed technique can be employed in any commercial FPGA and reconfigurable SoC with minimum speed and area over head.

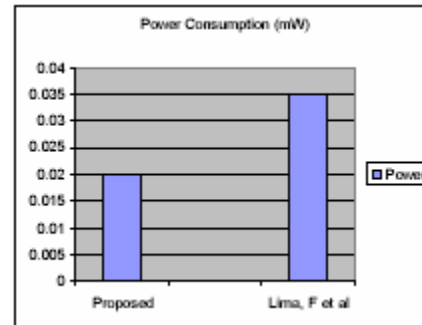


Figure 5: Power Analysis

## REFERENCES

- [1] <http://www.sti.nasa.gov/thesfrm1.htm>
- [2] K. Johansson, P. Dyreklev, B. Granbom, M.-C. Calvet, S. Fournier and O. Feuillat, "In-Flight and Ground Testing of Single Event Upset Sensitivity in Static RAMs," Accepted for publication IEEE Transactions on Nuclear Science
- [3] E. Normand, "Single Event Upset at Ground Level," IEEE Transactions on Nuclear Science, vol. 43, pp. 2742-2750, 1996.
- [4] J. Olsen, P. E. Becher, P. B. Fynbo, P. Raaby, and J. Schultz, "Neutron-Induced Single Event Upsets in Static RAMS Observed at 10 km Flight Altitude," IEEE Transactions on Nuclear Science, vol. 40, pp. 74-77, 1993.
- [5] Peterson, E.L., "Single-Event Analysis and Prediction", IEEE Nuclear and Space Radiation Effects Conference Short Course Text, 1997.
- [6] Massengill, L., "SEU Modeling and Prediction Techniques", IEEE Nuclear and Space Radiation Effects Conference Short Course Text, 1993.
- [7] Sexton, F.W., "Measurement of Single-Event Phenomena in Devices and ICs", IEEE Nuclear and Space Radiation Effects Conference Short Course Text, 1992
- [8] Lima, F., Carmichael, C., Fabula, J., Padovani, R., Reis, R., "A Fault Injection Analysis of Virtex® FPGA TMR Design Methodology", Proc. of (RADECS), Sept. 2001.
- [9] Carmichael, C., Fuller, E., Fabula, J., Lima, F., "Proton Testing of SEU Mitigation Methods for the Virtex FPGA", Proc. of MAPLD, 2001.
- [10] Dupont, D., Nicolaidis, M., Rohr, P., "Embedded Robustness IPs for Transient-Error-Free cs", IEEE Design and Test of Computers, May- June, 2002.
- [11] Lima, F., Carro, L., R., Reis, R., "Designing fault tolerant systems