

AN EFFICIENT FAULT TOLERANCE SCHEME FOR PREVENTING SINGLE EVENT DISRUPTIONS IN RECONFIGURABLE ARCHITECTURES

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ABSTRACT

Reconfigurable architectures are becoming increasingly popular with space related design engineers as they are inherently flexible to meet multiple requirements and offer significant performance and cost savings for critical applications. As the microelectronics industry has advanced, Integrated Circuit (IC) design and reconfigurable architectures (FPGAs, reconfigurable SoC and etc) have experienced dramatic increase in density and speed. These advancements have serious implications for the reconfigurable architectures when used in space environment where IC is subject to total ionization dose (TID) and single event effects as well. Due to transient nature of single event upsets (SEUs), these are most difficult to avoid in space-borne reconfigurable architectures. We present a unique SEU fault tolerance technique based upon double redundancy with comparison to overcome the overheads associated with the conventional schemes.

1. INTRODUCTION

Single event upset (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." [1]. SEUs are soft errors, and are non-destructive. An SEU may occur in analogue, digital, optical components, or may have effects in surrounding interface circuitry. Programmable Logic Devices (PLD), and more specifically Field Programmable Gate Arrays (FPGA), are replacing traditional logic circuits by offering the advantages of high integration (small size, low power, and high reliability) without the disadvantages of custom ASICs (high nonrecurring engineering cost and high risk, especially in limited production volume). Static Random Access Memories (SRAM) based FPGAs offer an additional unprecedented advantage. These can be reprogrammed for unlimited number of times, even in the end-user's system. In these FPGAs, a multitude of latches,

also called memory cells or RAM bits, define all logic functions and on-chip interconnects. Such latches are similar to the 6-transistor storage cells used in SRAMs, which has proved to be sensitive to single event upsets caused by high-energy neutrons [6]. The faults have been observed as bit errors in memories. The phenomenon has been observed at both aircraft altitudes and on ground [2][3][4][5], and is now considered an issue in the dependability of airborne electronics [3]. Many good summaries exist [6], [7], [8] that review these concepts in more detail. When an energetic ion passes through any material it loses energy through interactions with the bound electrons, causing an ionization of the material and the formation of a dense track of electron-hole pairs. The rate at which the ion loses energy is the stopping power (dE/dx). The incremental energy dE is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units of mg/cm^2 . The radiation effects community has adopted the term LET (Linear Energy Transfer) for the stopping power. An ion with an LET of 100 MeV-cm²/mg deposits approximately 1pC of electron-hole pairs along each micron of its track through silicon [15].

In this work, we propose a novel design technique to cope with radiation induced SEU faults in reconfigurable architectures. The proposed scheme is based on double hardware redundancy with comparison (DHRC). The scheme is evaluated by implementing it on a reconfigurable architecture proposed by the authors [13]. Different comparisons between contemporary schemes have been performed to benchmark the proposed scheme.

2. REDUCING TMR OVERHEADS BY USING DOUBLE HARDWARE REDUNDANCY

The TMR technique is a suitable solution for FPGAs because it provides a full hardware redundancy. However, it comes with some penalties because of its full hardware redundancy, such as area, I/O pads limitation and power dissipation. The amount of reliability required for critical applications such as space is normally accomplished through extra hardware or execution time. It is always a

need to make architectures more reliable with minimum extra components.

Aiming to reduce the overheads associated with a full hardware redundancy (TMR) and at the same time coping with the transient and permanent upsets, we present a new technique based on dual hardware redundancy with comparison (DHRC) to detect faults in programmable matrix (SEU in the programmable elements of reconfigurable architecture). The upset detection and voting section are implemented in hardware to eradicate faults and identify fault free block (correct value) to allow continuous operation of circuit. The main objective is to overcome drawbacks of full hardware redundancy (TMR). Moreover, it can present area reduction for some designs composed of large combinational logic structures.

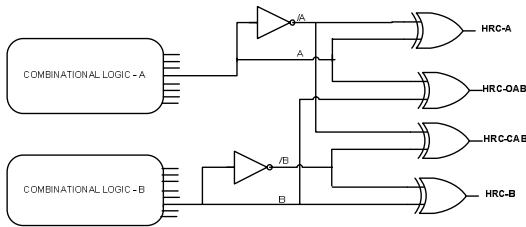


Figure-1: Dual Hardware Redundancy with Comparison

Figure-1 shows the details of the proposed scheme. As illustrated in the figure-1, there are two redundant blocks: A and B. Four values are captured through auxiliary exclusive OR gates. As a consequence, these four values are used to eliminate faulty block and help to identify correct fault free block. Two samples from each block are used in the proposed scheme: original and complemented. HRC-A: hardware redundancy comparator from block A. HRC-OAB: hardware redundancy comparator using original values from block A and B. HRC-B: hardware redundancy comparator from Block-B. HRC-CAB: hardware redundancy comparator using complemented values from Blocks A and B. Analyzing the sixteen possibilities of output combination of A, /A, B, /B. Eight different syndromes are recognized as presented in Table-1.

An upset in redundant block-A, syndrome 0011 & 1010, is characterized as a transient variation in the output with no changes in the block-B outputs. An upset occurrence in block-B is recognized in an equivalent way. There are many other syndromes that are not commonly seen in an ASIC environment, only in FPGAs. For example, the permanent effect of an upset syndrome 0000 & 1001. Analyzing these syndromes (0000, 1001), it is not possible to conclude which redundant block has the correct value. It has been proposed that when these permanent faults are detected in either of the blocks, the previous fault free value is considered and restored for continuous operation of the circuit.

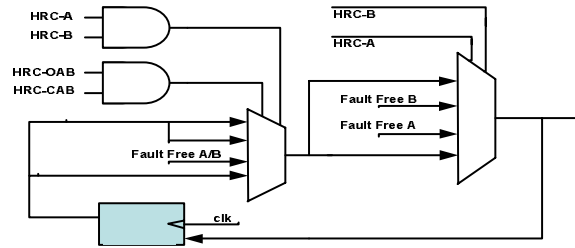


Figure-2: Voter circuit for the proposed scheme

The voter circuitry is implemented in hardware as shown in Figure-2. The voter takes into account the syndromes to evaluate fault free output in case of transient fault in either of redundant blocks. It has been proposed that the output pins may not be triplicated as the output already indicates the fault free value based on the proposed scheme. A synchronous element is used in the proposed scheme to hold the previous fault free value (Figure-3). This memory element can also be protected from SEU effects by incorporating a scheme already proposed by authors for synchronous elements of the circuit [14]. The proposed scheme along with scheme [14] by authors can be implemented on any commercially off the shelf available reconfigurable architecture for better area and power performance. Figure-3 illustrates implementation details of the proposed scheme.

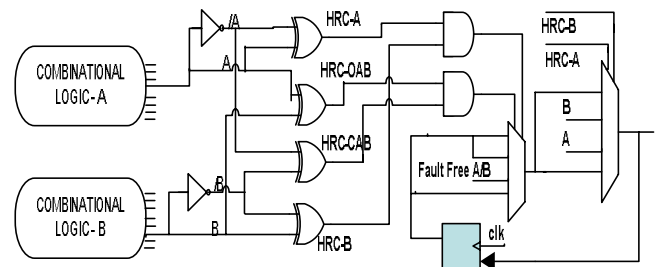


Figure-3: Implementation of the proposed scheme

3. EXPERIMENTAL SETUP AND RESULTS

We first elaborate the experimental flow which is incorporated for validating the proposed scheme. Then, we discuss the SEU simulator; we have developed to insert faults representing SEUs. We also discuss the functional testing procedure employed for accessing the SEU immunity of the proposed technique and, then we analyze the results by applying our unique technique.

The experiment flow involves following steps:

The proposed technique is coded in 'C' programme, which takes VERILOG net-list of the circuit under test as input. VERILOG net-list are obtained through Synplify_ASIC software. Logic blocks(clusters) are identified and structural modifications are made to the original circuit by modifying the net-list. The modified net-list is then fed into

software simulator to analyse the behaviour of the circuit under SEUs. The SEU immune net-list can be mapped on any ASIC/reconfigurable architecture (FPGA etc) through a suitable software tool (Xilinx Foundation Tool etc).

A SEU simulator is designed to create a realistic scenario for the faults to be injected into circuit under test due to SEU. The final step is to calculate Error. The circuit under test is introduced with SEU faults through SEU simulator. Figure-4 shows the process of error calculation. The functional operation of the proposed technique is compared with the original circuit with out SEU faults. A disparity between two circuits indicates that the SEU induced in the circuit has propagated to its outputs, thus leading to a functional failure. The SEU simulator is designed for the purpose of fault injection. The SEU simulator has these three main design considerations.

An SEU can occur on any line of the circuit. The fault can flip the logic value at any node. The SEU simulator is designed to randomly inject a SEU fault on any node/signal (0 to 1 or 1 to 0). An SEU can be of variable duration. When an SEU occurs at any node, it inverts the value on that line. The simulator allows the variation of SEU duration. The duration of SEU represents the period of fault injection. An SEU can occur at any instance during the functional operation of application. The SEU introduces fault on a line randomly in time. The SEU simulator has a special feature that it can induce multiple faults in addition to single event faults.

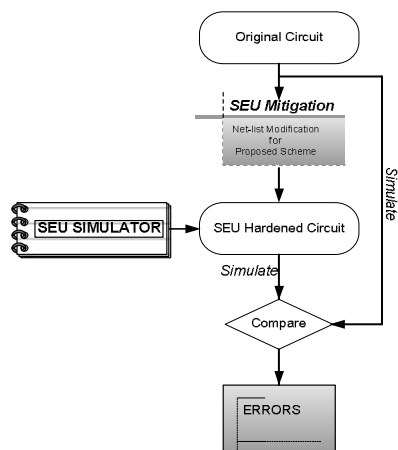


Figure-4: Error evaluation of the proposed technique

Let us take a case where line A has to be induced with an SEU. The line/node is assigned to one of the outputs of the simulator. The simulator assigns the original value on line A as fault-free value. A logic '1' on the simulator output driving line A will invert the original value during simulation. This value is denoted as fault-value.

SEU free block is identified with the help of the proposed scheme for the continuous operation of the circuit. In second scenario, the previous correct value is restored. This feature can be utilized to flag a permanent fault output

which may take any appropriate action while keeping the circuit in a legitimate state by restoring the previous correct value. Table-2 presents comparison results in terms of total number of Flip-Flops, combinational input pins and output pins of 2x2, 8x8, and 16x16 bit multipliers, using no tolerance scheme (standard), Fernanda, L. [8][9] scheme and the proposed scheme. It is quite clear from the results that approximately 40% reduction in number of Flip-Flops can be achieved through the proposed scheme. This reduction in number of Flip-Flops attributes to area, complexity and power savings. Moreover, approximately 67% output pins reduction is achieved as compared to contemporary techniques. Afore said savings make commercially off the shelf available reconfigurable architectures quite suitable for critical application like space application.

The synchronous part of the circuit to restore the previous correct value can be hardened against SEU through the scheme proposed by authors for synchronous elements [14].

4. CONCLUSION

This paper has described a new concurrent SEU mitigation technique for reconfigurable architectures. The proposed scheme gives immunity against all single faults. This technique reduces number of Flip-flops required for SEU immunity when compared with the previously proposed schemes. The proposed technique was validated by injecting random SEU with the help of SEU simulator. The fault injection procedure was developed in VERILOG, and it represents the effect of an SEU in a reconfigurable architectures. Experiment results illustrated that 100% of the faults can be detected with minimum hardware required. The proposed technique can be employed in any commercial FPGA and reconfigurable System on Chip (SoC) with minimum speed and area overhead.

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Table 1. Syndrome Analysis in the proposed scheme

A	/A	B	/B	HRC-OAB	HRC-A	HRC-B	HRC-CAB	Syndrome
0	0	0	0	0	0	0	0	Permanent Fault in Block-A or B
0	0	0	1	0	0	1	1	Transient Fault in Block-A
0	0	1	0	1	0	1	0	Transient Fault in Block-A
0	0	1	1	1	0	0	1	Permanent Fault in Block-A or B
0	1	0	0	0	1	0	1	Transient Fault in Block-B
0	1	0	1	0	1	1	0	No Fault
0	1	1	0	1	1	1	1	Transient Fault in Block-A or B
0	1	1	1	1	1	0	0	Transient Fault in Block-B
1	0	0	0	1	1	0	0	Transient Fault in Block-B
1	0	0	1	1	1	1	1	Transient Fault in Block-A or B
1	0	1	0	0	1	1	0	No Fault
1	0	1	1	0	1	0	1	Transient Fault in Block-B
1	1	0	0	1	0	0	1	Permanent Fault in Block-A or B
1	1	0	1	1	0	1	0	Transient Fault in Block-A
1	1	1	0	0	0	1	1	Transient Fault in Block-A
1	1	1	1	0	0	0	0	Permanent Fault in Block-A or B

Table 2. Comparison Results of the DHRC with other SEU Mitigation Techniques

	Standard			Fernanda, L Scheme[8][9]			Proposed Scheme		
	2x2	8x8	16x16	2x2	8x8	16x16	2x2	8x8	16x16
Multipier	4	16	32	8	32	64	8	32	64
Combinational Inputs	4	16	32	21	81	161	12	48	96
Number of Flip Flops	4	16	32	12	48	96	4	16	32
Output pins	4	16	32	12	48	96	4	16	32