Probability Based Partial Triple Modular Redundancy Technique for Reconfigurable Architectures

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Abstract—This paper represents a design technique for hardening combinational circuits mapped onto any reconfigurable architecture. An effective and simple algorithm for signal probabilities has been used to detect SEU sensitive gates for a given combinational circuit. The circuit can be hardened against radiation effects by applying triple modular redundancy (TMR) technique to only these sensitive gates. PTMR is tested against different circuits to prove its efficacy. With a small loss of SEU immunity, the proposed PTMR scheme can greatly reduce the area overhead as compare to TMR technique. PTMR scheme along with reconfiguration feature of FPGAs can result into a very effective SEU mitigation technique.

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1. INTRODUCTION

The possibility of single-event upsets was first postulated by Wallmark and Marcus in 1962[1]. The first actual satellite anomalies were reported by Binder et al. in 1975[2]. Some of the early pioneering work was by May and Woods, who investigated alpha-particle-induced soft errors[3]. In their work the source of alpha particles was not from space but rather from the natural decay of trace (parts/million) concentrations of uranium and thorium present in integrated circuit packaging materials. Single event phenomena can be classified into three effects (in order of permanency):

- Single event upset (soft error)
- Single event latch-up (soft or hard error)
- Single event burnout (hard failure)

Single event upset (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs."[4]. SEUs are soft errors, and are non-destructive. An SEU may occur in analogue, digital, optical components, or may have effects in surrounding interface circuitry.

Technology scaling, shrinking geometries into the deep sub-micron regime, lower supply voltages, higher operating frequencies, and higher density circuits have all had a negative impact on reliability. The number of occurrences of transient faults has increased dramatically. One major transient fault type is soft errors, caused by two main sources:

1) Secondary cosmic rays, especially atmospheric neutrons
2) Alpha particles emitted by decaying radioactive impurities in packaging and interconnect materials.

These highly energetic particles induce Single Event Transients (SET) in digital circuits. The amount of charge injected may be sufficient to invert the logical state at a node, hence introducing a soft error. Soft Error Rate(SER) per chip is projected to increase four times with decreasing feature size [5].

Traditionally, soft errors were tackled within the context of memory cells. Today, error detection and correction circuits are widely used to protect memory arrays. Combinational logic circuits, on the other hand, have been found to be less susceptible to SEU in equivalent device technologies due to the naturally occurring logical,

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[2]IEEEAC paper #1085, Version 4, Updated November 02, 2005

electrical and latching-window masking effects [6]. However, these phenomena are diminishing as feature size decreases and circuits move to higher operating frequencies. Recent studies predict that the soft error rate (SER) per chip of logic circuits will increase exponentially by year 2011, at which point it will be comparable to the SER per chip of unprotected memory elements [7].

For an SET, induced in a combinational logic circuit to result into a soft error, three conditions have to be satisfied:

a) An active path must exist between the hit node and the output of the circuit.
b) The pulse-width must be sufficient enough to avoid inertial delay filtration through subsequent gates, and survive electrical attenuation along the active path.
c) The pulse should arrive within the setup and hold time of a latch element to be captured and cause a soft fault [8].

In this work, we propose a novel design technique to cope with SEU related faults in combinational circuits. The design technique is based upon unique partial triple modular redundancy. SEU sensitive gates are identified on the basis of their input signal probabilities. A heuristic algorithm for detecting signal probabilities is used to calculate signal probabilities [9]. This proposed technique provides significantly better estimates for SEU sensitive gates than previously introduced techniques in literature.

2. SEU MECHANISM

Most of the research to date has concentrated on the effects of transient faults on flip-flops rather than the combinational logic. This is because transient faults, also know as Single Event Upsets (SEU), that occur in flip-flops are capable of changing the output state more readily, than faults in combinational circuits. Moreover, the ability of an SEU that occurs in combinational circuits to cause an error at the output of a flip-flop has been thought negligible.

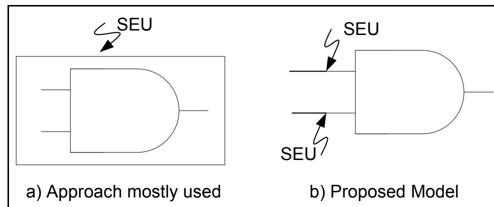

Figure-1 Proposed Model

SEU that occur in combinational circuits are due to a charged particle striking a small capacitance associated with the drain of a transistor that is off. This is known as Sensitive Volume. A charge build up produces a voltage transient that might then travel through the combinational logic to the input of a flip flop. An SEU that occurs in a combinational logic circuit must meet these conditions in addition to the reasons explained before, to cause an SEU at the output of a flip-flop.

a) A particle must strike the sensitive volume of a logic gate with sufficient energy to cause a transient with proper amplitude and pulse width for it to propagate through the circuit.
b) There should be a critical path from the incident gate to input of a flip-flop.
c) The transient must arrive in synchronisation with respective clock signal of flip-flop to cause an SEU.

3. MODEL DESCRIPTION

This probabilistic model calculates the soft error probability of any output node in a combinational circuit, based on logical masking principles.

The proposed approach differs from the ones found in the literature in three important ways:

1) This model assumes soft error hits at individual nodes, and not on the gate as a whole; this makes the model more realistic and accurate. (Figure-1)
2) The model accounts for input probabilities, i.e. it can accommodate unbalanced input vectors; this allows the designer to estimate soft error resiliency for specific input patterns, as well as random input patterns.
3) TMR is applied to only SEU sensitive gates.

Definitions: A gate input is sensitive if by complementing one of its input values, value changes at output. The input that controls the state of gate-output is defined hereby as dominant value. The sensitive input of a gate with two or more inputs is determined as follows:

a) If only one input has the dominant value, then gate is sensitive. (Figure-2a)
b) If all inputs have non dominant values, then all inputs are sensitive. (Figure-2b)

Since, we have signal probabilities rather than actual test vectors, in order to use the above definitions; we define a threshold probability as follows:
The logic value is assumed as logic‘0’ if its signal probability is less than threshold probability otherwise it is logic‘1’. This Threshold can be specified by end user depending upon the nature of application (Radiation Levels, etc).

For given threshold, logic values are assigned to each input, according to the criteria defined above. The gate’s sensitivity is then determined accordingly. The Algorithm, Dominate_Value(), shown in Figure-3 is employed to find the dominate value of gate inputs. If a gate has one or more sensitive inputs, then that gate is considered as sensitive to SEUs.

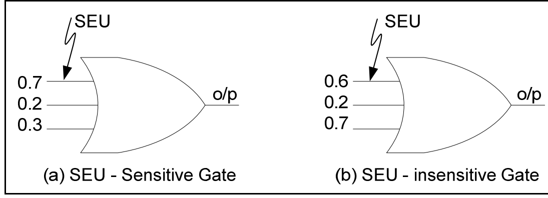

Figure-2 Proposed Model, SEU sensitive and insensitive gates

The signal probability of any output is calculated through a heuristic algorithm for estimating signal and detection probabilities [9].

Table-1 Signal Probabilities calculation formulas

Gate Type	Output Probability
AND	$\prod_i Pi$
NAND	$1-\prod_i Pi$
OR	$\sum_i Pi - \prod_i Pi$
NOR	$1-\left(\sum_i Pi - \prod_i Pi\right)$
XOR	$\sum_{i,j} P(i)(1-P(j))$
XNOR	$1-(\sum_{i,j} P(i)(1-P(j)))$

4. Case Example

Consider a 2-input AND gate with the signal probabilities of the inputs A and B equal to 0.4 and 0.6 and threshold probability as 0.5. According to the definitions described above, input A is at logic'0' and B at logic'1'. The dominant value is assigned to the gate inputs depending on its type. Let us now assume that a fault due to SEU is on one of the inputs 'A' at some instant of time, and assume that all other signals are at logic '1' at that instant. The fault propagates through the gate because all other signals are at non-dominant values.

```
1 Dominant_Value (Gate, Probability_Threshold,  dominant_value)
2 output: dominant_value
3 inputs: Gate, 0< Ptobability_Threshold <1
4 Determine Type of gate & dominant value
5    if (Gate is AND or NAND)
6         dominant value = FALSE;
7      elseif (Gate is OR or NOR)
8         dominant value = TRUE;
9 Return dominant value
```

Figure-3 algorithm to calculate Dominant Value

In other words a fault on the input A propagates to the output of the gate only when other inputs have non-dominant values. This can be defined in terms of probabilities as 'an SEU on one of the inputs of a gate has a higher probability of upsetting its output only if the signal probability of all other inputs being at non-dominant value is greater than or equal to the threshold probability'. Hence, the gate is assumed to be sensitive to SEUs on its inputs. Consider the 3-input AND gate with a different set of input probabilities, A (0.2), B (0.3), and C (0.9). The fault on line A has lesser probability of propagating through the gate as the probability of line B assuming non-dominant value is less than the threshold probability. Similarly the fault on line B or line C has a lesser chance of affecting the output of the gate consequently making the gate insensitive to SEUs. Algorithm Gate_sensitivity() determines gate sensitivity (Figure-4)

```
1 Gate_sensitivity (Gate, dominant_value, sensitive)
2 output: Gate sensitivity towards SEU TRUE/FALSE
3 inputs: Gate, dominant_value
4 for each input of Gate i
5    if i has dominant_value
6         then if rest of inputs have !dominant_value
7         then return TRUE
8          break
8    elseif only one of the rest inputs have dominant_value
9         then return TRUE
10        break
10   else return FALSE
11 end
```

Figure-4 algorithm to determine SEU sensitive gates

Triple Modular Redundancy is applied to only these SEU sensitive gates and to the gates at output stage of logic circuit irrespective of the fact that they are sensitive or no sensitive, as shown in figure-5a,b.

5. Estimation of Signal Probabilities

The detection probability of a given fault is the probability that a randomly chosen input vector detects the fault. The computation of detection probabilities of a given fault involves the computation of signal probabilities in the network. The signal probability of a line L in a network is the probability of line L having a value 1 on a randomly selected vector. Actually, the computation of the detection probabilities of a fault could be reduced to the computation of signal probability of an auxiliary gate, whose output is 1 if the sensitizing conditions of that fault are satisfied [10]. Consequently, the problem of computing the signal probabilities is of central importance in random pattern testability analysis.

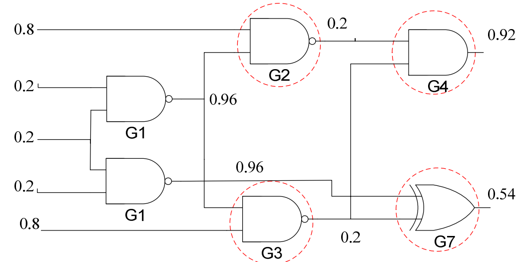

Figure-5a Logic circuit with input probabilities

The major difficulty in computing the signal probabilities is re-convergent fan-outs. In fact, if a circuit has no re-convergent fan-outs, then the independent formulas (table-l) used by the simple algorithm will compute the exact signal probabilities in a linear time. However, if a node has fans out greater than 1 and re-

converges at a gate input then the signal probability computation of the simple algorithm for all nodes driven by a gate is more likely to be deviated from the exact values.

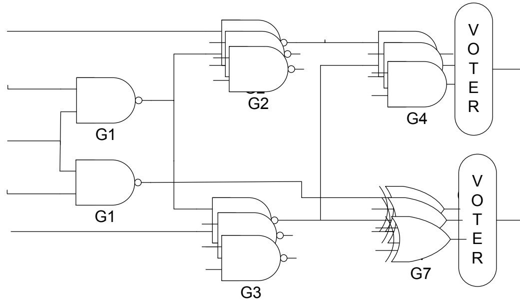

Figure-5b Partial TMR applied to only SEU sensitive gates

As the technique proposed is dependant upon the signal probabilities so it is very important that probabilities are calculated exact or as close to exact as possible in a reasonable time. The idea of our technique lies on calculation of signal probabilities which depends on observation that the deviated computation [9] of the simple algorithm for any gate could be caused by following reasons:

1) A re-convergence at gate
2) A re-convergence at a gate in its cone of influence
3) A combination of a and b.

The possibilistic algorithm distinguishes between these causes and uses a proper inference rule to reduce the error in every case. The technique for estimating signal probabilities [9] for every output gate is given in the following steps. (For the sake of clarity, the steps will be applied to the circuit in Figure-7.) Detailed explanation of the algorithm can be found in [9].

1) Estimate signal probabilities based upon (Table-1). These estimates are denoted by S.
2) Perform following procedure on each primary inputs of the logic circuit
   a) Compute signal probabilities by setting input I_i to 0 ($SP(I_i = 0)$).
   b) Compute signal probability by setting input I_i to 1 and, yielding the ($SP(I_i = 0)$). While performing step (a) and (b), all other inputs probabilities are set to ½.
   c) Compute the average of $SP(I_i = 0)$ and $SP(I_i = 0)$, denote the result as P-tuple (p).
3) For all gates, proceeding from the inputs to the outputs, perform the following steps:
   a) Compute the expected-tuple (E-tuple)[9] of each output gate using the P-tuples of its inputs using table-1.
   b) Mark Tuple (M-Tuple)[9] is calculated as explained by [9]. M-tuple gives cntrl_l and cntrl_2[9].
   c) Compute no-dependent (ND) value by using independent formulas (table-1) and the estimated signal probabilities of its inputs from previous level.
   d) Apply the inference rules listed in Figure-6.

```
Inference_Rules(cntrl_1, cntrl_2, P, S, ND)
2 output: Signal Probability
3 inputs: cntrl_1, cntrl_2, S (probability from table-1), ND
4 if cntrl_1 == 0 && cntrl_2 == 0
5     then P=S
6 elseif cntrl_1 != 0 && cntrl_2 == 0
7          then P = ND
8  elseif cntrl_1 == 0 && cntrl_2 !=0
9          if cntrl_2 == 1 then P = pi
10          else coeff = ∑(pi – ei)
11 P = ND + coeff + sign_of_coeff xcoeff / cntrl_2
12 endif
13  elseif cntrl_1 != 0 && cntrl_2 !=0
14          coeff = ∑(pi – ei)
15 P = ND + coeff + sign_of_coeff  * (S – ND) * coeff / S
16 endif
17 end
```

Figure-6 Inference Rules for estimation of Signa l Probability

An Illustrative Example

Consider the circuit shown in Figure-7. Different nodes are marked as a, b, …... First of all, signal probabilities are calculated through the algorithm explained above. The signal probabilities are shown in table-2. E-tuples and P-tuples are also shown in table-2 to clarify the complete process. Exact probabilities and calculated through table-1 are shown in table as well to show the efficacy of the technique.

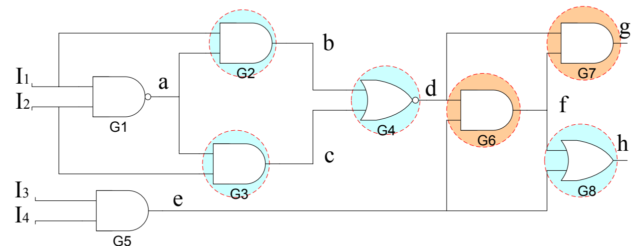

Figure 7: logical circuit with SEU sensitive gates

Dominant values are calculated through signal probabilities and SEU sensitive gates are detected. The Probability Threshold is assumed as 0.45 for this particular example.

The sensitive gates are encircled and shown in figure-7. Gates G6 and G7 (Figure-7) are not detected as sensitive gates if probability is calculated through table-1(most commonly used in literature). These two gates may effect SEU immunity of the circuit. Our proposed technique detects these gates as SEU sensitive gates. Exact probability figures are very close/same for different nodes as compare to simple probability calculation method Table-1). This interesting comparison authenticates the proposed technique.

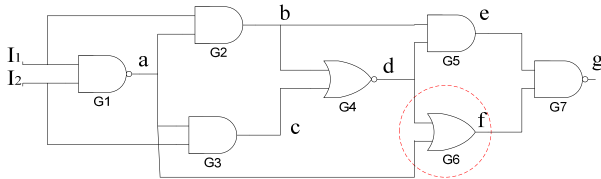

Figure-8 combinational circuit with SEU sensitive gates

A combinational circuit is shown in figure-8. Gate G6 is deduced as sensitive when considered normal probability projection method where as this gate is insensitive to SEU as calculated through proposed technique and through exact probabilities figure as well. Circuit in figure-7 is a good example to show that normal probability method can detect some gates as SEU sensitive which are inherently insensitive. Probability figures are shown in Table-3. This phenomenon can result into area overhead with out having any real advantage.

Table-2 Probabilty Calculations for reference circuit Figure-6

Nd	P-Tuple	E-Tuple	P	E	T
A	{0.75, 0.75 0.75, 0.75}	{0.75, 0.75 0.75, 0.75}	0.75	0.75	0.75
B	{0.25, 0.38 0.38, 0.38}	0.38, 0.38 0.38, 0.38	0.25	0.25	0.375
C	{0.38, 0.25 0.38, 0.38}	0.38, 0.38 0.38, 0.38	0.25	0.25	0.375
D	{0.44, 0.44 0.39, 0.39}	{0.47, 0.47 0.39, 0.39}	**0.53**	**0.5**	**0.391**
E	{0.25, 0.25 0.25, 0.25}	{0.25, 0.25 0.25, 0.25}	0.25	0.25	0.25
F	{0.11, 0.11 0.09, 0.09}	{0.11, 0.11 0.09, 0.09}	0.02	0.025	0.097
G	{0.05, 0.05 0.04, 0.04}	{0.05, 0.05 0.03, 0.03}	0.03	0.03	0.038
H	{0.33, 0.33 0.29, 0.29}	{0.33, 0.33 0.32, 0.32}	0.41	0.4	0.323

P= Proposed technique E = Exact Probability Model
T = Through Table-1 Nd = Node

Table-3 Probability Calculation for reference circuit figure-7

Node	Proposed Model	Exact Probability	Through Table-1
a	0.75	0.75	0.75
b	0.25	0.25	0.375
c	0.25	0.25	0.375
d	**0.525**	**0.5**	**0.391**
e	0.160	0.25	0.147
f	0.867	0.8	0.79
g	0.9749	0.95	0.88

TMR is only applied to a partial circuit as only sensitive gates are triplicated. The PTMR circuits is analysed through SEU simulator. The SEU simulator is designed in VERILOG. Simulator can inject faults of any duration and at any time which helps to fully analyse the proposed scheme. Results are shown in Table-4.

6. EXPERIMENTAL FLOW

The proposed technique is coded in 'C' programme, which takes netlist of the circuit under test as input. SEU-sensitive gates are identified and structural modifications are made to the original circuit. The modified netlist is then fed into software simulator to analyse the behaviour of the circuit under SEUs/SETs. The netlist can be mapped on any reconfigurable architecture (FPGA etc) through a suitable software tool (Xilinx Foundation Tool etc).

7. RESULTS

The Experimental results are derived for a medium sized circuit MCNC benchmark circuit c1355 and circuit shown in Figure-6 and 7. We injected random SEU, SET faults with duration of 3nsec, to verify our proposed scheme. Faults were injected through software simulations. Table-3 illustrates simulation results. Results are shown for original circuit with no TMR at all is indicated "original" in table-3. Results for proposed model are shown under the column heading of Proposed in table-3. And third main column shows results based upon commonly used techniques based upon table-1. Area saving is calculated as compared to standard TMR.

The results indicate that the proposed scheme has a area saving of approximately 14 to 17% for a small sized circuits. This area saving can be more/very significant for large circuits. The comparison of proposed scheme with ordinary probability projection model (table-1) confirms following points:

- Proposed scheme is more SEU immune
- Proposed scheme can be costly in terms of area but give better SEU fault coverage.
- Proposed scheme give approximately 97% SEU immunity

Table-4 Simulation Results with probability threshold = 0.45

Circuit	Original		Proposed		Table-1		
	E	A	E	A	E	A	Saving
Figure-6	63	8	9	20	19	16	16%
Figure-7	54	7	11	18	12	19	14%
C1355	99	82	8	202	14	319	17%

E = total number of times circuit is upset with SEU
A = Area overhead (# of gates),
Saving = area saving over standard TMR

8. CONCLUSION

This paper has described a new concurrent SEU/SET mitigation technique for combinational circuits. The proposed scheme gives significant immunity against all single faults. Results show that 95% to 97% SEU immunity can be achieved with an area saving of approximately 17%

for small sized circuits. The proposed technique can be employed in any commercial FPGA and reconfigurable SoC with minimum speed and area over head.

References

[1] J.T. Wallmark, S.M. Marcus, "Minimum size and maximum packaging density of non-redundant semiconductor devices," Proc. IRE, vol. 50, pp. 286-298, March 1962.

[2] D. Binder, E.C. Smith, A.B. Holman, "Satellite anomalies from galactic cosmic rays," IEEE Trans. on Nuclear Science, vol. NS-22, no. 6, pp. 2675-2680, Dec. 1975.

[3] T.C. May, M.H. Woods, “Alpha-particle-induced soft errors in dynamic memories”, IEEE Trans. On Electron Devices, vol.ED-26, no. 1, pp.2-9, Jan. 1979

[4]http://www.sti.nasa.gov/thesfrm1.htm

[5] P.Hazucha and C.Svensson. “Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate,” IEEE Transactions on Nuclear Science, Vol. 47, No. 6, pages 2586– 2594, Dec 2000.

[6] P. Liden, P. Dahlgren, R. Johansson, and J. Karlsson. “On Latching Probability of Particle Induced Transients in Combinational Networks,” Proceedings of the 24th Symposium on Fault-Tolerant Computing (FTCS-24), pages 340–349, 1994.

[7] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi. “Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic,” Proeedings of the.Inernational. Conference on Dependable Systems and Networks (DSN’02).

[8] L. W. Massengill, A. E. Baranski, D. O. V. Nort, J. Meng, and B. L. Bhuva. “Analysis of Single-Event Effects in Combinational Logic – Simulation of the AM2901 Bitslice Processor,” IEEE Trans. on Nuclear Science, 47(6):2609–2615, Dec 2000.

[9] Musaed A. Al-Kharji, Sami A. Al-Arian. "A New Heuristic Algorithm for Estimating Signal and Detection Probabilities," IEEE, glsvlsi, p. 26, 7th Great Lakes Symposium on VLSI, 1997.

[10]Savir, G. Ditlow, and P.H. Bardell, ” Random Pattern Testability” IEEE, Trans. Comp., vol. C-33, no. 1, pp.79-90, Jan. 1984.

Biography

Adrian Stoica is a Principal Member of Technical Staff in the Biologically Inspired Technology and Systems (BITS) Group in the Avionics Equipment Section at the Jet Propulsion Laboratory, California Institute of Technology. He obtained his MSEE degree from the Technical University of Iasi, Romania, ranking the first among the graduates in Applied Electronics Specialty. He received his Ph.D. in EECS from Victoria University of Technology in Melbourne, Australia, with a thesis titled “Motion learning by robot apprentices – a fuzzy neural approach”, which was the earliest work on humanoid robot motor skill learning by imitation. Since early 1986 his engineering and research work revolved around adaptive and learning techniques for autonomous intelligent systems. He joined JPL in 1996 where he has been working along two main themes: adaptive hardware for space autonomous systems, including evolvable/reconfigurable hardware, adaptive/learning hardware and sensor fusion hardware, and next-generation robots, focusing on rover intelligence and robot sensory-motor control. His current projects in reconfigurable and evolvable hardware address analog/digital field-programmable reconfigurable computing, automated hardware/software co-design and novel search/optimization techniques. Dr. Stoica initiated, and has chaired/co-chaired yearly since 1999, the NASA/DOD Conference in Evolvable Hardware, the main conference in the field of evolvable hardware as judged by number of attendants and references to published papers. He was Conference keynote speaker at ISMVL, ANNIE, gave tutorials at GECCO 2001 and CEC2003, and taught the first short course on Evolvable Hardware in the summer of 2003 at UCLA Extension. He has published over 100 papers in the areas of evolvable hardware, reconfigurable computing, fuzzy logic, neural networks, robot learning and is serving in the editorial board of several journals. He has received the 1999 JPL Lew Allen Award for Excellence (highest JPL award for excellence in research) and the Tudor Tanasescu Prize of the Romanian Academy in 2001.

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