Dynamically Reconfigurable NoC for Reconfigurable MPSoC

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ABSTRACT - **The performance of a Multiprocessor System-on-Chip (MPSoC) is not only dependent on the computational capabilities of on-chip processors but also depends on the communication medium connecting them. This has shifted the emphasis from computation to communication architectural design. In this paper, a dynamically reconfigurable Network-on-Chip (NoC) architecture has been proposed for reconfigurable MPSoC, as a solution to the increased communication needs, keeping low power, Quality of Service (QoS) and scalability of network in mind.**

I. INTRODUCTION

In early 1990s, John Cocke et. al. [1] argued that metal interconnections will be the limiting factor in achieving high performance from multiprocessor system. This prediction seems to hold existence in the future MPSoC, with a predicted System-on-chip (SoC) complexity of 4-billion transistors, built using 50-nm technology and running at 10GHz [2]. This enables the future SoCs to include RISC processors, DSP Cores, embedded DRAMs, flash memories, application specific hardware accelerators or RF components. In such complex systems, communication between the cores will become a major bottleneck due to limitations of the current bus based communication architecture. NoC is considered to be the solution to this communication issue.

This paper begins with looking briefly at the bus based communication system, reasons for the success of busses, NoC architecture is then discussed and finally a novel low power NoC architecture is proposed for MPSoC which is designed keeping high data throughput and scalability of network in perspective.

II. ONCHIP COMMUNICATION

Busses are widely used for on-chip communication. On-chip busses are mostly based on the ideas from standard PCB buses like VME and PCI. However the design for a SoC bus differs as it has to have faster transfer rate, shorter propagation delays and no restrictions on number of pins [3]. A simplest on-chip interconnect can be thought of just as a global bus shared by all the communicating nodes, for complex systems hierarchical buses are used. Different bus arbitration and handshaking techniques can be used for effective communication [4].

Buses have been deployed for communication since the beginning of circuit design and made their way in SoC due to their well understood concepts, their compatibility with most of the available node processors, the area taken on the chip and the zero latency after the arbiter has granted control.

Despite the advantages of buses, the bus based architecture will not meet the increased communication requirement because the bandwidth of a bus is shared by all the attached devices and it is simply not sufficient, firstly because the bus width cannot reasonably exceed a hundred bits, and secondly because the clocking frequency of global wiring becomes tightly constrained by the electrical properties of deep submicron processes [5]. Also every unit attached adds parasitic capacitance; therefore electric performance degrades with growth. Testability in bus based system is also problematic and slow.

For Future MPSoC, a new communication design paradigm is needed. This communication medium should aim to provide low power, reduce packet loss, utilize link efficiently, reduce contention and occupy less area on silicon.

NoC is considered to be the solution to this communication bottleneck. In NoC Each Processing Element (PE), abstracted as a node (Figure1), is connected to neighboring nodes by the micro network that can provide scalable and point to point concurrent connections. On- chip network architectures take their design concepts and methodologies from computer networks, especially from system area network and parallel computer cluster. However, NoC differ from the traditional network because of local proximity and because they are more predictable at design time. Energy constraint is another major difference.

On-chip communication is controlled by protocols (micro network stack) designed in layers, which is an adaptation of OSI seven layers scheme [6]. Different NoC architectures have been

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proposed based on different network topologies, routing algorithms, switching techniques and packet format [7][8][9].

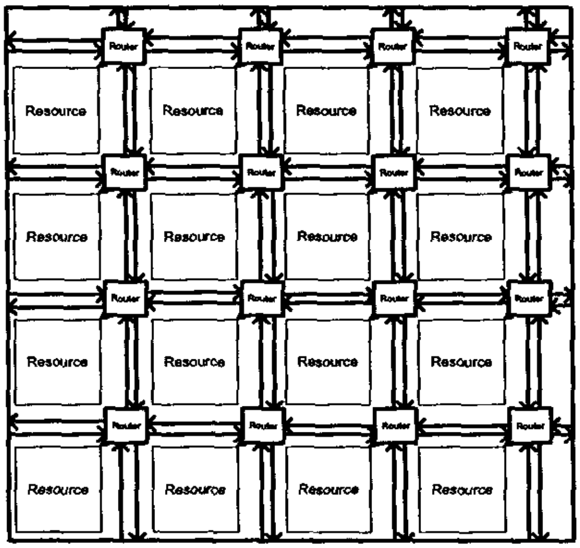

Figure1: A NoC with 16 nodes.

The fact that all the PEs in MPSoC has the ability to act as master makes the communication infrastructure design more challenging. For effective on-chip communication architecture, appropriate topology (how the channels are connected, Communication Protocols (exact manner in which communication across the channel take place), Architectural Parameters (properties of the channels and associated protocols), Clock speed (affected by placement of the various components, physical characteristics and routing of the wires) has to be considered.

III. PROPOSED NETWORK

Keeping in view the success of busses and communication requirements in MPSoC, we have proposed a Dynamically Reconfigurable NoC that combines the advantages of bus based systems and the advantages of NoC. The network changes its characteristics with the changing communication requirements of the system. The design inspiration comes from the fact that different PEs connected in a system have different bandwidth requirements. e.g., in an advance PDA with 3G communication capabilities, the on-chip communication can vary depending on the user application, thus network with fixed communication design parameters is not the optimal solution in terms of power and data throughput. The allocation of network resources depends on network topology, switching and routing decisions. Packet size also affects the network performance both in data throughput and overall system energy consumption [10].

In the Proposed design, the network configures itself in terms of its routing, switching and packet size to maintain the QoS requirement of system maintaining low power. The network is designed to cope with node failures by simply excluding the faulty node out of the communication system. Depending on redundancy of the data getting transferred, forward error correction and detection or error detection with retransmission is employed.

This intelligent network has its kernel in the form of micro network stack of the node processor. Depending on the data about to be transferred, the Micro Network Stack makes decision about the packet size, switching and routing, required for the data and includes this information in packet header. This information is read by the router and packets are processed as desired. Thus, in case of a PEs with high bandwidth requirements (Figure2), packet size would be increased, also switching would change from packet switching to circuit switching. These changes increases data throughput and decreases the switching power and timing delays. Distributed control of network has the advantage that if a single node failure occurs, the network continues to perform its functions.

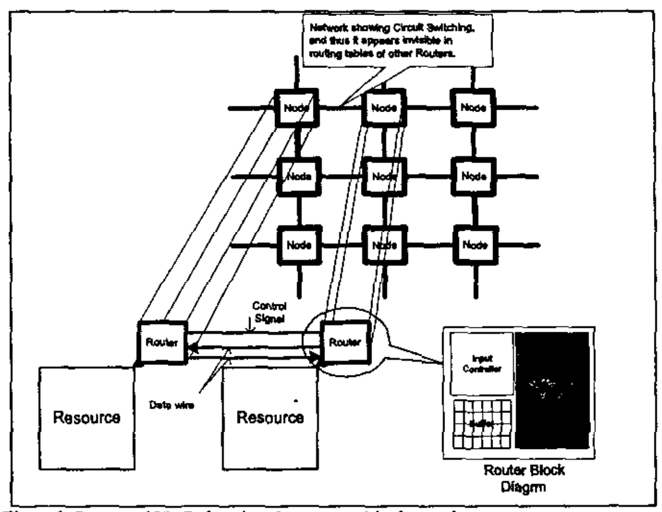

Figure2: Proposed NoC showing fragment with changed parameters.

Router is the main building block of the Network. It serves two main functions, Firstly; it acts as the interface between the PEs and network. To provide re-configurability, wrappers are used to provide interface for non compatible PEs. And secondly, it routes the data packets to the right path. In the proposed design, each router is connected to four neighboring routers. One of the important design constraints on router is to keep its silicon cost low, which is possible by keeping the internal buffer of router to as small as possible. In order to prevent packets queuing up internally in buffer, control signals are used to update routing tables for adaptive routing. Thus packets know in advance of coming to routers what the congestion is like, thus are routed to alternative paths to avoid having to queue up. This reduces the need for big internal data buffers. The proposed router has three important components, The Input Controller that manages the routing tables and determines the fate of arrived packets after its header inspection. Input Buffer that stores the incoming packet when it is getting inspected, and Switching Logic that connects the input ports to the output ports depending on the instructions from the Input Controller. Thus when a router is instructed to change mode to circuit switching, it informs its neighbors to exclude it from their routing table, and remembers the path established till it receives the end of transmission packet.

IV. NETWORK SIMULATION

In order to authenticate the proposed scheme, a Network Simulator NS-2 is used [11]. NS-2 is an object-oriented, discrete event driven network simulator developed at UC Berkely and is primarily useful for simulating local and wide area networks. NS-2 can be used to describe network topology, network protocols, routing algorithms and communication traffic generation in form of TCP and UDP. The simulator is written in C++ and OTcl. C++ is fast to run but slower to change, making it suitable for detailed protocol implementation. OTcl runs much slower but can be changed easily, making it ideal for simulation configuration.

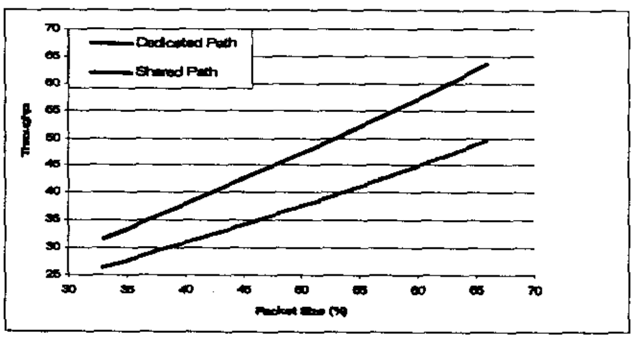

Figure3: comparison of data throughput vs packet size.

A network with 16 nodes in 4x4 torus topology is simulated. The aim of simulation is to investigate the effect of dynamically reconfiguration of network on data throughput. Channel between two PEs with high bandwidth requirement is investigated, first in a traditional packet switching context and compared with the dedicated (circuit switched) mode. In case of dedicated path, data throughput increased with the increase in packet size, however, in case of packet switched network, the data throughput doesn't increase in proportion as in case of dedicated path (Figure3). This is because no time is wasted in switching of packets in routers, also less time is spent on packet formation at the nodes. Thus, more data is transferred in same time. Less switching favors low power consumption as switching of packets consumes energy.

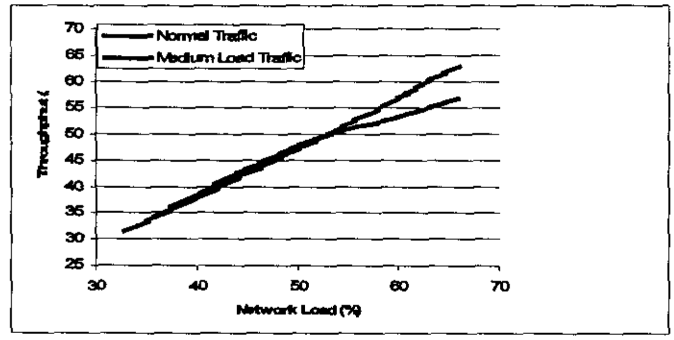

Figure4: comparison of data throughput vs packet size.

As explained in section III above, with the change in one part of network to circuit switching, this appears invisible to the rest of network, thus the traffic load is shifted to the other links. It is noticed that the links can accommodate 50% increase of load without any degradation to data throughput (Figure4), however, increasing it can affect the data throughput at receiving ends as bandwidth of channel is divided, this however is compensated by a slight increase in overall delivery time of data.

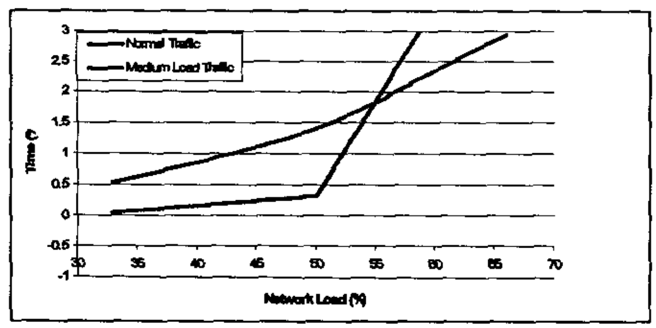

Figure5: Network load vs Time

In case of the standard packet switching network, with normal traffic of simple control signals or small memory transactions, increasing traffic load by 50% increases the data delivery time by 1.41% and the increase of 66% in traffic load increases the data delivery time by 2.9%. However, in case of medium load traffic involving frequent data exchange between the PEs, packet data time increases to 0.31% for 50% increase in traffic load, but drastically increase to 5.19 % for 66% increase of traffic load, thus badly affecting the QoS. This is where the proposed intelligent network takes the decision of dedicating a path for communication between the two PEs, i.e., changing the switching to circuit switching for that specific communication path. One would normally expected the time increase in case of normal traffic with increase in traffic load to show less increase in time but as seen in Figure5 above this is not the case. This is due to the fact that there is time wasted in making packets and more management work is done by the nodes. That is why the proposed network takes the idea of increasing the packet size to decrease the data delivery time.

Finally, the percentage increase in data throughput is compared with the type of traffic on network (Figure6), In case of Heavy load like multimedia traffic, the proposed network shows an increase of 65% throughput, and an increase of 63.5% from a normal packet switching network with few accesses to memory or transmission of control signals.

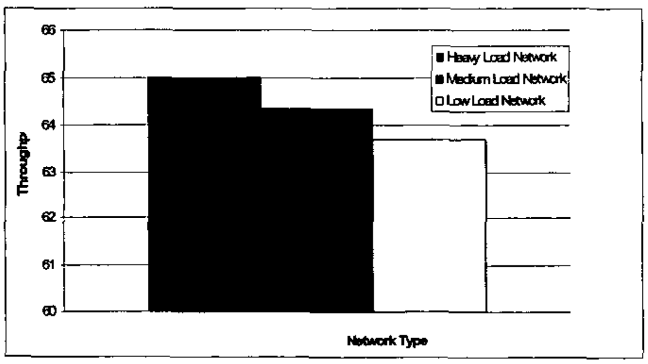

Figure6: comparison of data throughput vs Network Type.

V. CONCLUSION

This paper has briefly described the dynamically reconfigurable NoC, with intelligent nodes to change the communication parameters for high data throughput and less timing delays. The simulation results have demonstrated the effective use of network resources, making it a suitable alternative to traditional bus based MPSoC. The downside of this network in the form of complexity of its node is compensated by the increased data throughput and it is also expected to demonstrate low power utilization.

This kind of NoC can be ideal for MPSoCs with multimedia capabilities or for safety critical systems where the timing constraints are tight. Future work involves power and area optimization.

REFERENCES

1. H.S. Stone and J. Cocke. "Computer Architecture in the 1990s." Computer, Sept. 1991. Volume: 24, Issue: 9, page(s): 30 – 38.
2. International Technology Roadmap for Semiconductors web site http://public.itrs.net.
3. Dally W. and Towles B., "Route packets, not wires: Onchip interconnection networks." Design Automation Conference, 2001. Proceedings 18-22 June 2001 Page(s):684 – 689.
4. kyeong Keol Ryu, Eung Shin and Vincent J .Mooney, "A Comparison of Five Different Multiprocessor SoC BuS Architectures". (2001 IEEE).
5. Kamish Lahiri, Anand Raghunathan and Sujit Dey , "Evaluation of the traffic performance characteristics of System on Chip Communication Architectures".
6. J. Walrand, P. Varaiya, "High-Performance Communication Networks". Morgan Kaufman, 2000.
7. Shashi Kumar, et. al, "A Network on Chip Architecture and Design Methodology", IEEE Computer Society Annual Symposium on VLSI, Pittsburgh,Pennsylvania, USA, April 2002.
8. Pierre Guerrier, Alain Greiner, "A Generic Architecture for on-chip Packet-switched Interconnections".
9. Luca Benini, Giovanni De Micheli, "Network on Chips: A new SoC Paradigm", IEEE computer, Jan., 2002.
10. Luca Benini, Giovanni DE Micheli , "Powering Networks on Chips: Energy Efficient and Reliable interconnect design for SoCs."
11. The network simulator - ns-2, available at http://www.isi.edu/nsnam/ns/