Hybrid Communication Medium for Adaptive SoC Architectures

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Abstract

This paper proposes a hybrid communication medium for on-chip communication targeting adaptive SoC architectures. Unlike the work carried out in literature, where the term "hybrid" is used for the existence of more then one topologies for communication, the novelty of the proposed medium lies in combining two different communication media. In this paper, global bus and crossbars co-exist in an SoC. RFID Tag Reader is used as the targeted application and bus based system and crossbars based system implementation has been used for comparison purposes. RTL level implementation of the proposed communication structure is carried out for accurate power and area calculations. Results have demonstrated the effectiveness of hybrid communication medium over traditional bus and crossbars based SoC.

I. Introduction

Following Moore's law, system designers are now able to integrate many different types of IP blocks on a single chip. According to International Technology Roadmap for Semiconductors, by the end of this decade, System on Chips (SoCs), using 50-nm will grow to 4 billion transistors running at 10GHz [1]. The definition of a "system" in "system on a chip" has expanded to cover multiple processors, embedded DRAM, flash memory, application specific hardware accelerators, reconfigurable IP cores and RF components. This has created a situation where there is a mixture of traffic types utilizing the on-chip communication medium. The communication network that was traditionally handcrafted to a particular traffic type and constraints have to cope with additional burden now and proves to be a limiting factor in achieving the required performance from the present SoC.

A growing number of electronic systems are being designed with battery consideration in mind. Thus power consumption has become a crucial factor in determining the performance of the system. Interconnects have been shown to be a dominant source of power consumption in modern day SoC. This communication bottleneck has shifted the design paradigm from ccomputational centric to a communication centric design flow.

In this paper, we have investigated the use of hybrid communication medium, combining traditionally used bus and crossbars to address the issue of power and area faced in today's adaptive SoC design. This paper begins by looking briefly at the traditional bus and crossbars based systems in section II, this is followed by the related work done in field of hybrid communication medium in section III. Section IV describes the targeted platform. The proposed hybrid architecture and implementation of targeted system using alternative communication media is discussed in section V. Finally section VI describes our power and area results obtained by implementation of a SoC system.

II. Background

Buses have been deployed for communication since the beginning of circuit design and made their way in SoC due to their well understood concepts, their compatibility with most of the available node processors, the area taken on the chip and the zero latency after the arbiter has granted control. Most of the recent designs of on-chip buses borrow their ideas from standard PCB buses. A lot of work in literature has been carried out on bus based systems and to cope with the changing technology requirements, new bus architectures have been evolved. Kyeong et al. [2] has given a good comparison of the different bus architectures.

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Despite the advantages of buses, the bus based architecture will not meet the increased communication requirement because the bandwidth of a bus is shared by all the attached devices and it is simply not sufficient, firstly because the bus width cannot reasonably exceed a hundred bits, and secondly because the clocking frequency of global wiring becomes tightly constrained by the electrical properties of deep submicron processes [3]. Also every unit attached adds parasitic capacitance; therefore electric performance degrades with growth. Testability in bus based system is also problematic and slow.

A crossbar switch network is used for communications switching and for computer interconnection. It is a non blocking network. In the two-sided crossbar switch, there is only one path between every pair of IPs. Crossbars provide a high data throughput alternative to buses. A lot of work has been carried out in communication through crossbars and many different designs have been evolved targeting increased data throughput and fault tolerance [4] [5].

The basic principles of low power design include [6] [7]:

- Reduce switching voltage
- Reduce voltage swing
- Reduce capacitance
- Reduce switching frequency
- Reduce leakage and static currents

All of these factors are related to each other in one way or another and hence changing one affects the other, thus a compromise has to be reached. Yan Zhang and M J Irwin, compared power and performance of crossbars and buses for on-chip interconnect and have concluded that crossbars consumes more energy per cycle, incurs more delay than a bus, and therefore has a larger energy-delay product per cycle. However, since an N x N crossbars can accommodate up to N non-conflicting data transfers per cycle, it has a much larger throughput. Although more energy is consumed in one cycle, crossbars has smaller energy consumption per bit of data transfer. As a result it also has a smaller energy-delay product per transfer than a bus when the number of input/output ports is small and it operates in full parallelism. But crossbars pay a large penalty in area [8].

In our work presented in this paper, we have combined the high data throughput crossbars with a global bus for an SoC system and has compared its area and power with the traditional implementation scenario of just using bus and crossbars.

III. Related Work

Literature search lists a lot of work carried out in the field of on-chip communication from bus based systems [2] [3] to complex NoCs [9]. However no work is done where two different communication structures with different power and throughputs are co-existed in same SoC. The term hybrid communication is so far only limited when combining two different topologies in a same communication medium. E.g. R. Huang and R. Vemuri [10] have proposed a hybrid interconnect structure which takes advantages of both mesh and tree topologies, but no power analysis have been presented.

We have targeted RTL level simulation of IP Cores in a system with a hybrid communication system, where crossbars and bus co-exist, emphasising on power and area.

IV. Platform Description

In order to demonstrate the proposed hybrid communication medium, an example of Radio Frequency Identification (RFID) Tag Reader is considered. The RFID tag contains a transponder with a digital memory chip that possesses a unique ID, and an antenna to send and receive data to a reader. The RFID tag reader consists of an antenna, transceiver and decoder. The reader generates a continuous activation signal, and when a tag is within range of this signal, the tag sends the reader its identification.

Upon signal detection and identification of the tag, the tag reader then sends command signals to it. Responding to commands from the reader, the tag sends out encoded data. This data, which is sent out on a modulated frequency, is picked up and decoded by the reader, which sends it to a host computer to be processed.

The main components of the RFID include the RF antenna part, A/D converter interface, cryptography module, UART, keypad module (input), Data coding(Manchester encoding used for demo), controller that checks the output of encoder against output of cryptography module, Memory module (to hold list of users and the pins) and the display module to display user details [11].

V. Implementation Scenario

For comparison purposes, three basic implementation scenarios are considered,

- Using Global Bus
- Using Crossbar switch
- And using a hybrid communication medium that is crossbars and global bus in same system.

A. GLOBAL BUS STRUCTURE

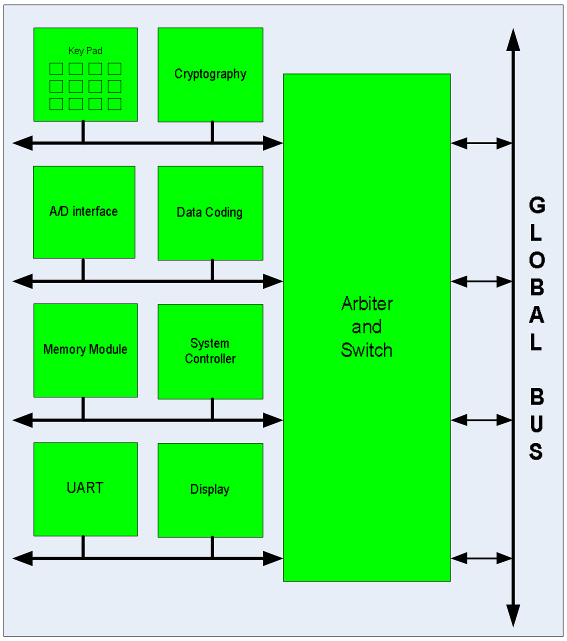

Figure 1. RFID Reader System based on a global bus.

In Global Bus architecture, a single bus is shared by all the IPs in a system. An arbiter is used to grant access of the bus to the IP. This access can be granted in FIFO or in Round Robin fashion.

Figure 1 shows the RFID modules connected by a Global Bus. The placement of IPs on the bus is made keeping in mind the master and slave relationship of the IPs. Master refers to a data transmitting IP that initiates the communication and slave refers to the receiver. A point to point link is used between IPs that needs to communicate only with each other and hence decreasing the communication on the global bus. This arrangement ensures the global bus is available more frequently when required. Arbitration is implemented in Round Robin fashion.

The advantage of this bus is in terms of its simple structure and widely understandable concepts. However, this comes at the cost of speed of the system as only one IP can transmit data on the bus at any given time, making other IPs wait till the transaction is completed so they can get access of the bus [02].

B. CROSSBARS STRUCTURE

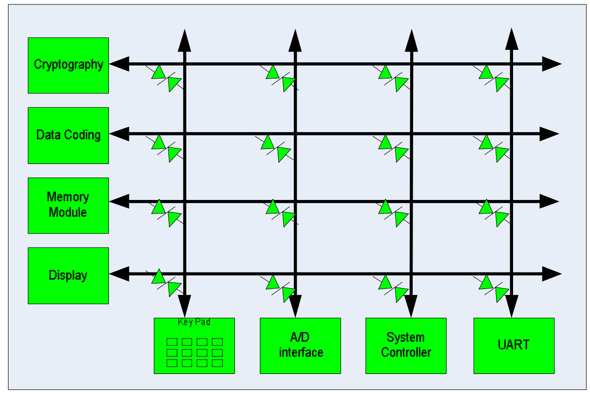

Figure 2. RFID Reader System with Crossbar switch.

The Second implementation scenario considered is using a crossbar switch. A crossbar switch is capable of channelling data between any two IP modules that are attached to it up to its maximum number of ports. The paths set up between IPs can be fixed for some duration or changed when desired and each IP-to-IP path (going through the switch) is usually fixed for some period.

Figure 2 shows the implementation of RFID system using crossbars. As in case of last scenario, care has been taken during placement of IPs to make sure the path between IPs that need to communicate more with each other are not blocking access of other inter IP communication.

Crossbars topology can be contrasted with bus topology, an arrangement in which there is only one path that all IPs share. A major advantage of crossbars switching is that, as the traffic between any two IPs increases, it does not affect traffic between other modules. In addition to offering more flexibility, a crossbar switch environment offers more scalability than a bus environment [12].

C. HYBRID INTERCONNECT

The third scenario considered is a hybrid structure that utilises crossbars and global bus in a same SoC. R. Huang and R. Vemuri [10] investigated the effect of utilising hybrid interconnect (both mesh and tree topologies) in an FPGA based system and concluded that the proposed model of hybrid interconnect can significantly reduce the routing area and achieve high performance. The aim of our hybrid implementation is to exploit the advantages of hybrid interconnects (cross bar and global bus) in a system and see its effect on power and area.

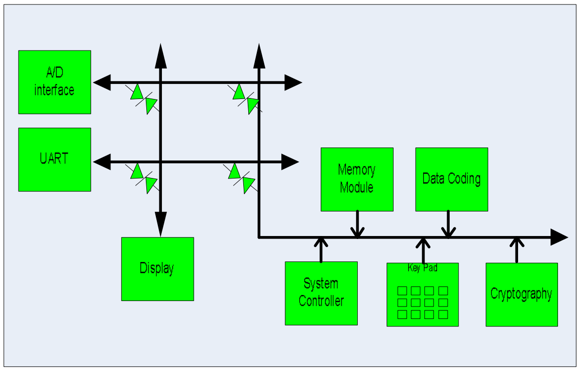

Figure 3. RFID Reader System with Hybrid Interconnect.

Placement of IPs.

Figure 3 shows the implementation of RFID system by hybrid interconnects. Placement of IPs in the system is based on the communication requirement of the respective IPs. In the proposed design, the IPs connected to the crossbars are categorized as Masters and can establish communication with any IPs in the system. For example, A/D converter module takes inputs from the user and its output is used by Display module, system controller, cryptography and data coding. Hence it is classified as Master and is placed on the crossbars so it can communicate effectively without having to wait for the arbiter to give access to the global bus. However, the IPs on the global bus act as both Master and slave. The effectiveness of this interconnect scheme can be fully utilized if high data throughput IPs are placed in same cluster close to their communication partners and not at different communication structures. This thus stops from keeping the global bus engaged and making other IPs wait for their transaction to complete.

The arbiter implemented for the hybrid network performs a complex task of dealing with allocation of both crossbar links and global bus to the IP wanting access. Hence, the area of the arbiter is increased (results in next section).

VI. Comparison Results

Hardware gate level simulation is carried out and Synopsys design compiler is used to calculate power and area of different scenarios considered. 0.18 micron technology library is used for ASIC synthesis.

Table 1. IP CORES AREA OVERHEAD AND POWER CONSUMPTIONS

IP-CORE	AREA (CELL)	TOTAL DYNAMIC POWER (mW)	CELL LEAKAGE POWER (uW)
UART	5724.329590	2.6891	0.4369
Memory	10541.980469	7.5413	1.2998
Keypad	1935.150024	0.4403	0.1729
Display	3768.709961	0. 7753	0.4193
AES	94231.929688	0. 3069	0.0439
A/D Interface	19766.849609	13.0557	2.1388
System Control	25723.926151	15.738	4.6231
Encoder	16845.497162	9.2341	1.8251
Bus	3183.199951	1.2950	0.3352
Crossbars	9033.290039	0.8189	0.1948
Hybrid	7183.359863	2.4465	0.8159

Table 1 shows the individual power and area calculations of the IPs and communication medium. Figure 4 shows the total power of the system when employed using the three chosen communication media. It can be seen that we get the least power when global bus is employed as a communication medium for the system. This is because of the fact that in bus based system only one IP is effectively communicating with other IPs for a system at any given time; hence global bus gives the least power figures. Also the bus arbiter is simple and grants bus access to the IP in lesser clock cycles. This however comes at a cost of less data throughput due to single IP communication at any given time.

Another aspect considered for comparison is area of the system. Figure 5 shows the total area of the system when implemented using different communication scenarios. As shown in the graph, when crossbar is employed for communication, the area of system increases. This also correlates with the conclusion drawn by the author in [08]. The increased power consumption of crossbars shown in Figure 4 is at any given time due to more data being communicated at any given time.

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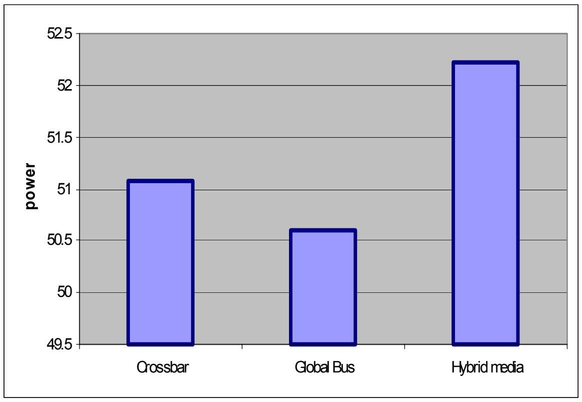

Figure 4. Overall Power Consumption of System with Different Communication Media.

A compromise has to be reached between power and area figures when choosing the best performer. From the results obtained, hybrid communication medium appeared to be the best performer. The area is slightly more then global bus but less then the crossbars. However, the power figures obtained clearly shows the effectiveness of the hybrid system in combining advantages of both bus and crossbars. Just to emphasise that the power figure shown in the Figure 4 are at any given clock cycle and not per data transfer. As more data is getting transferred per clock cycle thus overall power increases. Another factor that contributes to this increase in power is the need for more complex switching for communication between the IPs on different channels.

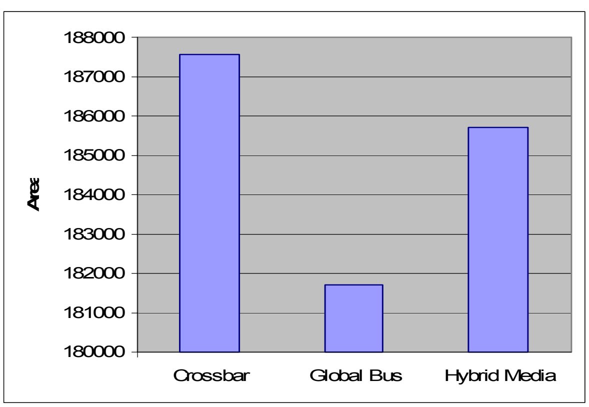

Figure 5. Area Overhead of System with Different Communication Media.

The crossbars part of system can increase the communication due to the possibility of simultaneous IP communication, thus increasing the power of system. The increase in area is because of the complex arbiter needed to effectively utilize the medium. Hybrid implementation also has an advantage in placement that it gives us flexibility to place high communicating IPs together and thus utilize the advantages of crossbars, and by placing low communicating IPs on global bus we get the advantage of buses like getting quicker access to bus to finish the communication task etc.

VII. Conclusion

In this paper, we have proposed a novel hybrid communication medium for adaptive SoC, combining bus and crossbars. Hardware implementation carried out in Verilog shows the effectiveness of the proposed medium when demonstrated using RFID Tag reader as case study. Hybrid communication medium gives us less power per amount of data transfer (overall power at any clock cycle is increased due to more data getting transfer at any given clock cycle), when compared with same system implemented using bus and crossbars. The area utilized by the hybrid medium is again less then crossbar implementation proving its effectiveness at that front as well.

The next phase of our work targets power and area analysis of adaptive SoC architectures with other communication media involving NoC, AMBA bus, etc..

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