

2011 NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2011)



June 6 – 9, 2011

**San Diego Convention Center
San Diego, California, USA**

Organized by

NASA Jet Propulsion Laboratory (JPL), European Space Agency (ESA),
University of Edinburgh, UK

Supported by

Society for Adaptive and Evolvable Hardware and Systems (ADEVO)
Bio-Inspired Technologies and Systems (BITS), -JPL
IEEE Circuits and Systems Society (IEEE-CAS)
ACM Special Interest Group on Design Automation (ACM-SIGDA)

General Chair

David Merodio, *European Space Agency (ESA), Netherlands*

Vice General Chairs

Tughrul Arslan, *The University of Edinburgh, UK*
Umeshkumar Patel, *Goddard Space Flight Center, USA*



MONDAY, JUNE 6, 2011

TUTORIALS

Chair: Ahmet Erdogan, University of Edinburgh, UK
Room 28CD

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|---------------|---|
| 8:30 - 9:30 | Tutorial 1: Design of Analog-to-Digital Converters with Adaptive Resolution <i>M.B. Srinivas</i> <i>Birla Institute of Technology and Science, India</i> |
| 9:30 - 10:30 | Tutorial 2: Integrated System Health Management (ISHM): Enabling Intelligent Systems <i>Fernando Figueroa</i> <i>NASA Stennis Space Center, USA</i> |
| 10:30 - 11:00 | BREAK Room 28E |
| 11:00 - 12:00 | Tutorial 3: Adaptive Sensing in Smart and Intelligent Sensor Systems <i>Sergey Y. Yurish</i> <i>International Frequency Sensor Association, Spain</i> |
| 12:00 - 13:00 | Tutorial 4: Building reconfigurable hardware for Space using commercial-off-the shelf FPGAs: challenges and possible solutions <i>Massimo Violante, Politecnico di Torino, Italy</i> <i>Fernanda Lima Kastensmidt, Federal University of Rio Grande do Sul (UFRGS), Brazil</i> |
| 13:00 - 14:00 | LUNCH (on your own) and DAC Exhibition |
| 14:00 - 15:00 | DAC Keynote: Up Close and Personal with Steve Wozniak Speaker: Steve Wozniak - Fusion-io, San Jose, CA Room: 20AB |
| 15:15 - 16:15 | Tutorial 5: Adaptive Embedded System Design and Verification: Challenges & Solutions <i>Bhanu Kapoor, Mimasac, USA</i> <i>Shireesh Verma, Conexant, USA</i> <i>Prapanna Tiwari, Synopsys, USA</i> <i>John Goodenough, ARM, UK</i> |
| 16:15 - 17:45 | Tutorial 6: Command & Control Buses as enabler for modular, reconfigurable spacecrafts: present & future <i>Gianluca Furano</i> <i>European Space Agency (ESA), Netherlands</i> |
| 17:45 - 18:45 | Tutorial 7: Catastrophic Damage from Total Dose in Space and Potential Recovery Methods <i>Allan Johnston</i> <i>NASA JPL, USA</i> |

| DAY 1 - TUESDAY, JUNE 7, 2011 Day Chair: Didier Keymeulen, JPL, USA Room 28CD | |
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| 8:30 - 10:00 | DAC Keynote Megatrends Driving Embedded Multicore Innovation Speaker: Lisa Su - Freescale Semiconductor, Inc., Austin, TX <i>Room: 20AB</i> |
| 10:00 - 10:20 | BREAK Room 28E |
| 10:20 - 10:40 | Welcome Address and Organisational Remarks David Merodio, European Space Agency (ESA), Netherlands Didier Keymeulen, Jet Propulsion Laboratory (JPL), USA |
| 10:40 - 11:40 | Invited Keynote Address Tunneling through the technology barrier: Thinking small to get the biggest change in space capability Dr. Steven C. Suddarth Director of the Configurable Space MicroSystems, Innovations and Applications Center (COSMIAC), USA Chair: Adrian Stoica, Jet Propulsion Laboratory (JPL), USA |
| | Session A. Reconfigurable computing incl. multi core architectures Chair: Didier Keymeulen, Jet Propulsion Laboratory (JPL), USA |
| 11:40 - 12:00 | 11 - MAESTRO: Orchestrating Predictive Resource Management in Future Multicore Systems <i>Sangyeun Cho and Socrates Demetriades</i> <i>University of Pittsburgh, United States</i> |
| 12:00 - 12:20 | 37 - Resource Optimization and Deadlock Prevention while Generating Streaming Architectures from Ordinary Programs <i>Lei Gao, Gaurav Mittal, David Zaretsky, and Prith Banerjee</i> <i>Binachip Inc., United States</i> |
| 12:20 - 14:00 | LUNCH (on your own) and DAC Exhibition |
| 14:00 - 14:20 | 45 - Multicore SoC for On-Board Payload Signal Processing <i>Karel H.G. Walters¹, Sabih H. Gerez², Gerard J.M. Smit², Sebastien Baillou², Gerard K. Rauwerda², and Roland Trautner³</i> ¹ University of Twente, Netherlands ² Recore Systems, Netherlands ³ European Space Agency (ESA), ESTEC, Netherlands |
| 14:20 - 14:40 | 92 - Unifying Manycore and FPGA Processing with the RUSH Architecture <i>Brandon Beresini¹, Scott Ricketts¹, and Michael Bedford Taylor²</i> ¹ Maxentric Technologies, United States ² Angstromush, United States |
| | Session B. Reconfigurable and morphable hardware Chair: David Merodio, European Space Agency (ESA), Netherlands |
| 14:40 - 15:00 | 75 - Maximizing the Accuracy of Sound Based Tracking via a Low-Cost Network of Reconfigurable Embedded Nodes <i>Varun Subramanian, Anurag Umbarkar, and Alex Doboli</i> <i>State University of New York at Stony Brook, United States</i> |
| 15:00 - 15:20 | 71 - Reconfigurable Analog VLSI Circuits for Robot Path Planning <i>Scott Koziol and Paul Hasler</i> <i>Georgia Institute of Technology, United States</i> |
| 15:20 - 15:40 | 77 - Optically Reconfigurable Gate Array with a Polymer-Dispersed Liquid Crystal Holographic Memory <i>Takayuki Mabuchi¹, Minoru Watanabe¹, Akifumi Ogiwara², and Fuminori Kobayashi³</i> ¹ Shizuoka University, Japan ² Kobe City College of Technology, Japan ³ Kyushu Institute of Technology, Japan |
| 15:40 - 16:00 | BREAK Room 28E |
| 16:00 - 16:20 | 52. Research on Design Method of Scalable Configurable IP Core <i>Lei Li, Jian Wang, Yuan Wang, and Jinmei Lai</i> <i>Fudan University, China</i> |
| 16:20 - 16:40 | Session C. Built-in self-test and self-repair Chair: Umeshkumar Patel, Goddard Space Flight Center, USA |
| | 62 - UNITRONICS: A Novel Bio-Inspired Fault Tolerant Cellular System <i>Mohammad Samie, Gabriel Dragffy, and Tony Pipe</i> <i>University of the West of England, UK</i> |
| 16:40 - 17:00 | 66 - Application-Aware Optimization of Redundant Resources for the Reconfigurable Self-Healing eDNA Hardware Architecture <i>Michael Reibel Boesen, Jan Madsen, and Paul Pop</i> <i>Technical University of Denmark, Denmark</i> |
| 17:00 - 17:20 | 32 - Radiation Hardening By Design: A Novel Gate Level Approach <i>Massoud Mokhtarpour Ghahroodi¹, Mark Zwolinski¹, and Emre Ozer²</i> ¹ University of Southampton, United Kingdom ² ARM Ltd, United Kingdom |
| 17:20 - 18:00 | BREAK |

| 18:00 - 21:00 | Reception and Posters Chair: Ahmet Erdogan, University of Edinburgh, UK Room 28E |
|---------------|---|
| Poster 1 | 80 - Optimizing High Speed Serial Communication Using Honeywell Rad Hard SerDes Gary Roosevelt, Weston Roper, and Thomas Romanko Honeywell Microelectronics, United States |
| Poster 2 | 44 - Exploratory Study about the Use of New Reconfigurable FPGAs in Space Rafal Graczyk ¹ , Marcin Stolarski ¹ , and Patrick Cormery ² ¹ Space Reserch Center of Polish Academy of Sciences, Poland ² EADS Astrium, France |
| Poster 3 | 56 - AMBA to SoCWire Network on Chip Bridge as a Backbone for a Dynamic Reconfigurable Processing Unit Holger Michel ¹ , Frank Bubenhagen ¹ , Björn Fiethe ¹ , Harald Michalik ¹ , Björn Osterloh ² , Wayne Sullivan ³ , Alex Wishart ³ , Jørgen Ilstad ⁴ , and Sandi Alexander Habinc ⁵ ¹ IDA TU Braunschweig, Germany ² DSI GmbH, Germany ³ Astrium Ltd, UK ⁴ European Space Agency (ESA), Netherlands ⁵ Aeroflex Gaisler AB, Sweden |
| Poster 4 | 57 - Application-Driven Dimensioning of a Coarse-Grain Reconfigurable Array Waqar Hussain, Tapani Ahonen, Fabio Garzia, and Jari Nurmi Tampere University of Technology, Finland |
| Poster 5 | 47 - Area Efficient Processing Element Architecture for Compact Hash Functions Systems on VIRTEx5 FPGA Platform Mohamed El-Hadedy, Danilo Gligoroski, and Svein Johan Knapskog Norwegian University of Science and Technology, Norway |
| Poster 6 | 49 - FPGA Implementation of K-means Algorithm for Bioinformatics Application: An Accelerated Approach to Cluster Microarray Data Hanaa M. Hussain ¹ , Khaled Benkrid ¹ , Huseyin Seker ² , Ahmet T. Erdogan ¹ ¹ The University of Edinburgh, United Kingdom ² De Montfort University, United Kingdom |
| Poster 7 | 31 - A Technique for the Identification of Reconfigurable Resources of Flexible Communication Systems Jiong Ou, Farooq Muhammad, Jan Haase, and Christoph Grimm Vienna University of Technology, Austria |
| Poster 8 | 58 - An FPGA Task Allocator with Preliminary First-Fit 2D Packing Algorithms Chuan Hong ¹ , Khaled Benkrid ¹ , Xabier Iturbe ^{1,2} , Ahmet T. Erdogan ¹ , Tughrul Arslan ¹ ¹ The University of Edinburgh, United Kingdom ² IKERLAN, Spain |
| Poster 9 | 72 - A Self-Configurable Computing Architecture for Unstructured and Unknown Reconfigurable Fabrics Avinash Amarnath and Christof Teuscher Portland State University, United States |
| Poster 10 | 78 - Hybrid CMOS/Nanoelectronic Circuits for High Throughput Pattern Matching Applications Fabien Allbart, Timothy Sherwood, and Dmitri B. Strukov University of California Santa Barbara, United States |
| Poster 11 | 69 - Toward Generic and Adaptive Avionic Test Systems George Afonso ¹ , Rabie Ben Atitallah ² , Nicolas Belanger ³ , Martial Rubio ³ , Stephan Stilkerich ¹ , Jean-Luc Dekeyser ⁴ ¹ EADS IW/INRIA Lille Nord Europe, France ² LAMIH, UVHC, INRIA Lille-Nord Europe, France ³ Eurocopter Group, France ⁴ LIFL, USTL, INRIA Lille-Nord Europe, France |
| Poster 12 | 42 - Energy-Aware Video Coding of Multiple Views via Workload Balancing Domenic Forte and Ankur Srivastava University of Maryland, United States |
| Poster 13 | 87 - Integration of the Self-Healing eDNA Architecture in a Liquid Crystal Waveguide-based Fourier Transform Spectrometer Michael Reibel Boesen ¹ , Didier Keymeulen ² , Jan Madsen ¹ , Thomas Lu ² , Tien-Hsin Chao ² ¹ Technical University of Denmark, Denmark ² Jet Propulsion Laboratory, United States |
| Poster 14 | 33 - eTissue: A Bio-Inspired Match-based Reconfigurable Hardware Architecture Supporting Hierarchical Self-healing and Self-evolution Jiaqing Xu ¹ , Yong Dou ¹ , Qi Lv ¹ , and Jing Zhang ² ¹ National University of Defense Technology, China ² Virginia Polytechnic Institute and State University, United States |
| Poster 15 | 55 - Application of an Adaptive Digital Controller for Medium Power Satellite DC/DC Converter Konrad R. Skup, Paweł Grudziński, Piotr Orleński Space Research Centre PAS, Poland |
| Poster 16 | 82 - Embedded High Speed Model Predictive Controller on a FPGA Koldo Basterretxea ¹ and Khaled Benkrid ² ¹ University of the Basque Country (UPV/EHU), Spain ² The University of Edinburgh, United Kingdom |
| Poster 17 | 61 - A Fast Reconfigurable 2D HW Core Architecture on FPGAs for Evolvable Self-Adaptive Systems Andrés Otero ¹ , Rubén Salvador ¹ , Javier Mora ¹ , Eduardo De la Torre ¹ , Teresa Riesgo ¹ , Lukáš Sekanina ² ¹ Universidad Politécnica de Madrid, Spain ² Brno University of Technology, Czech Republic |
| Poster 18 | 51 - An FPGA-based Parameterised and Scalable Optimal Solutions for Pairwise Biological Sequence Analysis Mohd Nazrin Md Isa, Khaled Benkrid, Thomas Clayton, Cheng Ling, and Ahmet T. Erdogan The University of Edinburgh, United Kingdom |
| Poster 19 | 79 - Fault Tolerant Three-Dimensional Cellular Genetic Algorithms with Adaptive Migration Schemes Asmaa Al-Naqi, Ahmet T. Erdogan, and Tughrul Arslan The University of Edinburgh, United Kingdom |
| Poster 20 | 40 - High Performance Intra-task Parallelization of Multiple Sequence Alignments on CUDA-compatible GPUs Cheng Ling, Khaled Benkrid, and Ahmet T. Erdogan The University of Edinburgh, United Kingdom |
| Poster 21 | 36 - A High Performance Implementation for Molecular Dynamics Simulations on a FPGA Supercomputer Server Kasap ¹ and Khaled Benkrid ² ¹ Cyprus International University, Turkey ² University of Edinburgh, United Kingdom |
| Poster 22 | 54 - High Performance Linear Equation Solver Using NVIDIA GPUs Yoon Kah Leow, Ali Akoglu, Ibrahim Guven, and Erdogan Madenci University of Arizona, United States |

| DAY 2 - WEDNESDAY, JUNE 8, 2011 Day Chair: Luca Fossati, European Space Agency (ESA), Netherlands Room 28CD | |
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| 08:30 - 9:30 | Invited Keynote Address: Exascale computing - an impossible challenge? Dr. Mark Parsons EPCC (Edinburgh Parallel Computing Centre), The University of Edinburgh, UK Chair: David Merodio, European Space Agency (ESA), Netherlands |
| | Session D. Special Session on Dynamically Reconfigurable Embedded Systems Chair: Giovanni Beltrame, Ecole Polytechnique de Montreal, Canada |
| 09:30 - 09:50 | 86 - Concepts, Architectures, and Run-time Systems for Efficient and Adaptive Reconfigurable Processors <i>Lars Bauer, Muhammad Shafique, and Jörg Henkel</i> <i>Karlsruhe Institute of Technology (KIT), Germany</i> |
| 09:50 - 10:10 | 60 - Run-Time Resource Instantiation for Fault Tolerance in FPGAs <i>Monica Magalhaes Pereira¹, Lars Braun², Michael Hübner², Jürgen Becker², and Luigi Carro¹</i> ¹ Universidade Federal do Rio Grande do Sul, Brazil ² Karlsruhe Institute of Technology, Germany |
| 10:10 - 10:30 | 90 - A Heterogeneous SoC Architecture with Embedded Virtual FPGA Cores and Runtime Core Fusion <i>Peter Figuli, Michael Hübner, Romuald Girardey, Falco Bapp, Thomas Bruckschlägl, Florian Thoma, Jörg Henkel, and Jürgen Becker</i> <i>Karlsruhe Institute of Technology, Germany</i> |
| 10:30 - 10:50 | 67 - Enabling FPGA Systems for Future Deep Space Exploration Missions: Improving Fault-Tolerance and Computation Density with R3TOS <i>Xabier Iturbe¹, Khaled Benkrid¹, Tughrul Arslan¹, Chuan Hong¹, Ahmet T. Erdogan¹, and Imanol Martinez²</i> ¹ The University of Edinburgh, United Kingdom ² IKERLAN-IK4 Research Alliance, Spain |
| 10:50 - 11:00 | BREAK Room 28E |
| 11:00 - 12:00 | DAC Keynote - The Imminent EDA Transformation Speaker: Gadi Singer - Intel Corp., Santa Clara, CA Room 20AB |
| 12:00 - 14:00 | LUNCH (on your own) and DAC Exhibition |
| | Session E. Reconfigurable Hardware for Space Applications Chair: Michael Newell, Jet Propulsion Laboratory (JPL), USA |
| 14:00 - 14:20 | 85 - The Future of Embedded Systems at ESA: Towards Adaptability and Reconfigurability <i>Luca Fossati and Jorgen Iltad</i> <i>European Space Agency, Netherlands</i> |
| 14:20 - 14:40 | 70 - Real-Time Estimates of Differential Signal Phase for Spaceborne Systems Using FPGAs <i>Vishwas Vijayendra, Paul Siqueira, Hari Krishnan Chandrikakutty, Akilesh Krishnamurthy, and Russell Tessier</i> <i>University of Massachusetts, United States</i> |
| 14:40 - 15:00 | 50 - Analysis of SEU Effects in Partially Reconfigurable SoPCs <i>Luca Sterpone¹, Fabio Margaglia², Markus Koester², Jens Hagemeyer², Mario Porrmann²</i> ¹ Politecnico di Torino, Italy ² University of Paderborn, Germany |
| 15:00 - 15:20 | BREAK Room 28E |
| | Session F. Adaptive Hardware/Software for Autonomous Systems Chair: Luca Fossati, European Space Agency (ESA), Netherlands |
| 15:20 - 15:40 | 59 - Failure Management for Cost-Effective and Efficient Spacecraft Operation <i>Enrico Noack¹, Tino Noack², Vijay Patel³, Ingo Schmitt², Mark Richters¹, Johannes Stamminger¹, Sonja Sievi¹</i> ¹ Astrium GmbH, Germany ² TU Cottbus, Germany ³ ITP Engines UK Ltd., United Kingdom |
| 15:40 - 16:00 | 41 - Adaptable Video Compression and Transmission using Lossy and Workload Balancing Techniques <i>Domenic Forte and Ankur Srivastava</i> <i>University of Maryland, United States</i> |
| | Session G. Adaptive Embedded Systems: Design and Implementation Chair: Michael Newell, Jet Propulsion Laboratory (JPL), USA |
| 16:00 - 16:20 | 83 - A Runtime Adaptive Controller for Supporting Hardware Components with Variable Latency <i>Christian Pilato, Vito Giovanni Castellana, Silvia Lovergine, Fabrizio Ferrandi</i> <i>Politecnico di Milano, Italy</i> |
| 16:20 - 16:40 | 7 - A Post-Manufacturing Language-Adaptive Embedded Processor System <i>Yong-Kyu Jung</i> <i>Gannon University, United States</i> |
| 19:00 - 22:00 | Conference Cruise Dinner and Prize Awards Board at San Diego Marriott Marina, GATE 3, from 6:45 PM – 7 PM |

| DAY 3 - THURSDAY, JUNE 9, 2011 Day Chair: Umeshkumar Patel, Goddard Space Flight Center, USA Room 28CD | |
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| 08:30 - 09:30 | Invited Keynote Address: Adapting remote systems: Getting it right the second time Robert Manning Mars Science Laboratory (MSL) Flight System Chief Engineer, Jet Propulsion Laboratory, USA Chair: Didier Keymeulen, Jet Propulsion Laboratory (JPL), USA |
| 09:30 - 10:40 | DISCUSSION PANEL Adaptive Systems for Future Moderator: Adrian Stoica, Jet Propulsion Laboratory (JPL), USA |
| 10:40 - 11:00 | BREAK Room 28E |
| 11:00 - 12:00 | DAC Keynote - Cognitive Computing: Neuroscience, Supercomputing, Nanotechnology Speaker: Dharmendra S. Modha - IBM Research - Almaden, San Jose, CA Room 20AB |
| 12:00 - 14:00 | LUNCH (on your own) |
| | Session H. Special Session on New Frontiers in the Unsupervised Evolution of FPGA-based Circuits Chairs: Marco D. Santambrogio (MIT) and Fabio Cancare (Politecnico di Milano) |
| 14:00 - 14:20 | 88 - A Bird's Eye View of FPGA-based Evolvable Hardware <i>Fabio Cancare¹, Sheetal Bhandari², Davide Basilio Bartolini¹, Matteo Carminati¹, and Marco Domenico Santambrogio^{1,3}</i> ¹ Politecnico di Milano, Italy ² International Institute of Information Technology, India ³ Massachusetts Institute of Technology, United States |
| 14:20 - 14:40 | 89 - Evolvable Systems on Reconfigurable Architecture via Self-Aware Adaptive Applications <i>Filippo Sironi¹, Andrea Cuoccio¹, Henry Hoffmann², Martina Maggio^{1,2}, and Marco Domenico Santambrogio^{1,2}</i> ¹ Politecnico di Milano, Italy ² Massachusetts Institute of Technology, United States |
| 14:40 - 15:00 | 64 - Evolvable 2D Computing Matrix Model for Intrinsic Evolution in Commercial FPGAs with Native Reconfiguration Support <i>Ruben Salvador¹, Andrés Otero¹, Javier Mora¹, Eduardo de la Torre¹, Teresa Riesgo¹, Lukas Sekanina²</i> ¹ Universidad Politecnica de Madrid, Spain ² Brno University of Technology, Czech Republic |
| 15:00 - 15:20 | 43 - Evolutionary Design of Efficient and Robust Switching Image Filters <i>Zdenek Vasicek¹, Michal Bidlo¹, Lukas Sekanina¹, Kyrre Glette²</i> ¹ Brno University of Technology, Czech Republic ² University of Oslo, Norway |
| 15:20 - 15:40 | BREAK Room 28E |
| | Session I. On-chip Learning and Adaptation Chair: Niels Hadaschik, Fraunhofer Institute for Integrated Circuits IIS, Germany |
| 15:40 - 16:00 | 53 - A Workload-Aware Neuromorphic Controller for Dynamic Power and Thermal Management <i>Saurabh Sinha, Jounghyuk Suh, Bertan Bakkaloglu, and Yu Cao</i> Arizona State University, United States |
| 16:00 - 16:20 | 63 - An Adaptive Fuzzy Logic-based Routing Algorithm for Networks-on-Chip <i>Masoud Dehyadegari¹, Masoud Daneshtalab^{1,2}, Masoumeh Ebrahimi², Juha Plosila², Siamak Mohammadi¹</i> ¹ University of Tehran, Iran ² University of Turku, Finland |
| 16:20 - 16:40 | Concluding Remarks |

AHS-2011 Conference Dinner on Wednesday, June 8, 2011

*****Boarding Location*****

We will be boarding at the Marriott Marina, located at 333 West Harbor Drive. The boarding gate is GATE 3. Boarding will take place from 6:45 PM – 7:00 PM. Please make sure that you board by 7:00 PM as that is the departure time. Contact person is Jacquelyn Campbell, direct line is (619) 686-8700.

Itinerary

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|---------------------|---|
| 06:45 pm - 07:00 pm | Board at San Diego Marriott Marina, GATE 3 |
| 07:00 pm - 09:45 pm | Cruise |
| 09:45 pm - 10:00 pm | Dock and Disembark at Marriott Marina, GATE 3 |

